12/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0016625589 - Drawing available
WPI ACC NO: 2007-340526/200732
Related WPI Acc No: 2007-891164
XRPX Acc No: N2007-251548
Integrated circuit interconnections testing method for electronic system, involves applying alternating current stimulus to alternating current coupled interconnection during run-state/idle controller state
Patent Assignee: CISCO TECHNOLOGY INC (CISC-N)
Inventor: BAEG S H; CHUNG S S
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 7174492 B1 20070206 US 2001834506 A 20010412 200732 B

Priority Applications (no., kind, date): US 2001834506 A 20010412

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 7174492 B1 EN 23 16

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...having a plurality of voltage transitions;scanning an initiate AC test instruction into the instruction **register** of both ICs;performing an execute AC test instruction by moving the TAP controller to the Run-Test/Idle state and holding the **TAP controller** of **both** ICs in the Run-Test/Idle state for the time required to complete execution of...
Basic Derwent Week: 200732

12/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0016365710 - Drawing available
WPI ACC NO: 2007-081880/200708
Related WPI Acc No: 2002-673401
XRPX Acc No: N2007-056935
Multi-core processing apparatus consists of test access port controller in each processor core, which is selected dynamically for controlling distributed test control mechanism
Patent Assignee: MINER D E (MINE-I); MURRAY S W (MURR-I); TU S J (TUSJ-I)
Inventor: MINER D E; MURRAY S W; TU S J
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 20060248426 A1 20061102 US 2000746676 A 20001222 200708 B
US 2006477837 A 20060629

Priority Applications (no., kind, date): US 2000746676 A 20001222; US 2006477837 A 20060629

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 20060248426 A1 EN 15 9 Continuation of application US 2000746676

Alerting Abstract ...NOVELTY - A multi-core processor comprises a **test access port controller** (TAPC) in **each** processor core and test access port (TCP) configuration **registers** in a non-processor core. The TAPCs and the configuration **register** are coupled through integrated test buses (114, 124). One of the TAPCs is dynamically selected...

Original Publication Data by Authority

ArgentinaBasic Derwent Week: 200708

12/3,K/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2008 The Thomson Corporation. All rts. reserv.

0014345598 - Drawing available
WPI ACC NO: 2004-533810/200451
XRPX Acc No: N2004-422789
Test access port controllers coupling method in integrated circuit, involves selecting test access port controller based on state of bit in controller, and coupling selected controller's terminals to external terminals
Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); US PHILIPS CORP (PHIG)
Inventor: STEINBUSCH O
Patent Family (10 patents, 106 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
WO 2004057357	A1	20040708	WO 2003IB5950	A	20031215	200451	B
AU 2003288584	A1	20040714	AU 2003288584	A	20031215	200474	E
EP 1579229	A1	20050928	EP 2003780425	A	20031215	200563	E
			WO 2003IB5950	A	20031215		
JP 2006510980	W	20060330	WO 2003IB5950	A	20031215	200623	E
			JP 2004561840	A	20031215		
US 20060090110	A1	20060427	WO 2003IB5950	A	20031215	200629	E
			US 2005539104	A	20050615		
CN 1729401	A	20060201	CN 200380106839	A	20031215	200643	E
KR 2005084395	A	20050826	WO 2003IB5950	A	20031215	200644	E
			KR 2005711239	A	20050617		
EP 1579229	B1	20061122	EP 2003780425	A	20031215	200677	E
			WO 2003IB5950	A	20031215		
DE 60309931	E	20070104	DE 60309931	A	20031215	200705	E
			EP 2003780425	A	20031215		
			WO 2003IB5950	A	20031215		
DE 60309931	T2	20070913	DE 60309931	A	20031215	200761	E
			EP 2003780425	A	20031215		
			WO 2003IB5950	A	20031215		

Priority Applications (no., kind, date): US 2002435395 P 20021220

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 2004057357	A1	EN	22	6	

National Designated States, Original: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NI NO NZ OM PG PH PL PT RO RU SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW

Regional Designated States, Original: AT BE BG BW CH CY CZ DE DK EA EE ES FI FR GB GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT RO SD SE SI SK SL SZ TR TZ UG ZM ZW

AU 2003288584	A1	EN		Based on OPI patent WO 2004057357
EP 1579229	A1	EN		PCT Application WO 2003IB5950
				Based on OPI patent WO 2004057357

Regional Designated States, Original: AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

JP 2006510980	W	JA	17	PCT Application WO 2003IB5950
				Based on OPI patent WO 2004057357
US 20060090110	A1	EN		PCT Application WO 2003IB5950
KR 2005084395	A	KO		PCT Application WO 2003IB5950
				Based on OPI patent WO 2004057357
EP 1579229	B1	EN		PCT Application WO 2003IB5950
				Based on OPI patent WO 2004057357

Regional Designated States, Original: AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PT RO SE SI SK TR

DE 60309931	E	DE		Application EP 2003780425
				PCT Application WO 2003IB5950
				Based on OPI patent EP 1579229

			Based on CPI patent WO 2004057357
DE 60309931	T2	DE	Application EP 2003780425
			PCT Application WO 2003IB5950
			Based on CPI patent EP 1579229
			Based on CPI patent WO 2004057357

Original Titles:
CONNECTING **MULTIPLE TEST ACCESS PORT CONTROLLERS** THRCUGH A SINGLE TEST ACCESS PORT...

...CONNECTING **MULTIPLE TEST ACCESS PORT CONTROLLERS** THRCUGH A SINGLE TEST ACCESS PORT...

...CONNECTING **MULTIPLE TEST ACCESS PORT CONTROLLERS** THRCUGH A SINGLE TEST ACCESS PORT...

...Connecting **multiple test access port controllers** on a single test access port...

...CONNECTING **MULTIPLE TEST ACCESS PORT CONTROLLERS** THRCUGH A SINGLE TEST ACCESS PORT...

Alerting Abstract ...NOVELTY - An initial bit of **each test access port** (**TAP**) **controllers** (102, 106), is reset to a specific state. A signal is output based on the state of bit in the controllers. A TAP controller is selected based on the signal. The external input...
...ADVANTAGE - **Several TAP controllers** are accessed without using additional chip pins, by adding single bit to data register of...

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
Multiple test access port (**TAP**) **controllers** on a single chip are accessed, while maintaining the appearance to an outside observer of having only a single test access port controller. By adding a single bit to a data **register** (212) of **each** of a plurality of **TAP controllers** (102, 106), along with straightforward combinational logic, the **plurality** of **TAP controllers** can be accessed without the need for additional chip pins, and without the need for **additional TAP controllers**. **Toggling** the state of the added **bits** in the respective data **registers** of the **plurality** of **TAP controllers** provides the control information for either selecting one TAP controller or daisy-chaining of the **plurality** of **TAP controllers**.

Multiple ...

...Multiple test access port (TAP) controllers on a single chip are accessed, while maintaining the appearance to an outside observer of having only a single test access port controller. By adding a single bit to a data register (212) of each of a plurality of TAP controllers (102, 106), along with straightforward combinational logic, the plurality of TAP controllers can be accessed without the need for additional chip pins, and without the need for additional TAP controllers. Toggling the state of the added bits in the respective data registers of the plurality of TAP controllers provides the control information for either selecting one TAP controller or daisy-chaining of the plurality of TAP controllers.

...

... **Multiple test access port** (**TAP**) **controllers** on a single chip are accessed, while maintaining the appearance to an outside observer of having only a single test access port controller. By adding a single bit to a data **register** (212) of **each** of a plurality of **TAP controllers** (102, 106), along with straightforward combinational logic, the **plurality** of **TAP controllers** can be accessed without the need for additional chip pins, and without the need for **additional TAP controllers**. **Toggling** the state of the added **bits** in the respective data **registers** of the **plurality** of **TAP controllers** provides the control information for either selecting one TAP controller or daisy-chaining of the **plurality** of

TAP controllers .

Claims:
...A method of coupling a plurality of test access port , TAP , controllers (102, 106) that each comprise a one-bit register (212) for storing a first register bit to a single external interface, comprising: a) resetting the first register bit in the one- bit register (212) of each of plurality of TAP controllers (102,106) to a known state;b) producing a first signal (216);c) selecting one of the plurality of TAP controllers (102, 106) based, at least in part, on the first signal;d) coupling an external input terminal (TDI) to an input terminal of the selected one of the plurality of TAP controllers (102, 106); ande) coupling an output terminal (TDO) of the selected one of the plurality of TAP controllers (102, 106) to an external output terminal;characterized by producing the first signal (216) based, at least in part, on the state of the first register bit in each of the plurality of TAP controllers (102,106...

...What is claimed is:1. A method of coupling a plurality of test access port (TAP) controllers to a single external interface, comprising: resetting a first bit in each of plurality of TAP controllers (102, 106) to a known state; producing a first signal based, at least in part, on the state of the first bit in each of the plurality of TAP controllers (102, 106); selecting one (108) of the plurality of TAP controllers based, at least in part, on the first signal; coupling an external input terminal to an input terminal of the selected one of the plurality of TAP controllers ; and coupling an output terminal of the selected one of the plurality of TAP controllers to an external output terminal. ...Basic Derwent Week: 2003WO-IB0005950

12/3,K/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0014240100 - Drawing available
WPI ACC NO: 2004-426136/200440
XRPX Acc No: N2004-338417
Multi-processor system has processors respectively connected to debug execution units, which are selected by selector for performing debugging
Patent Assignee: RENESAS TECH CORP (RENE-N); RENESAS TECHNOLOGY CORP (RENE-N); RENESAS TECHNOLOGY KK (RENE-N)
Inventor: HAYASE K
Patent Family (3 patents, 3 countries)
Patent Application
Number Kind Date Number Kind Date Update
JP 2004164367 A 20040610 JP 2002330310 A 20021114 200440 B
US 20040163012 A1 20040819 US 2003654893 A 20030905 200455 E
CN 1501250 A 20040602 CN 200310114386 A 20031114 200465 E

Priority Applications (no., kind, date): JP 2002330310 A 20021114

Patent Details
Number Kind Lan Pg Dwg Filing Notes
JP 2004164367 A JA 16 7
Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...When only the CPU (70) is to be debugged, a TAP controller (100) sets a register (101) so that a signal (S11) is "H" and a signal (S12) is "L." When only the CPU (71) is to be debugged, the TAP controller (100) sets the register (101) so that the signal (S11) is "L" and the signal (S12) is "H." When both CPUs (70) and (71) are to be debugged, the TAP controller (100) sets the register (101) so that the signals (S11) and (S12) are both "H."
Claims: Basic Derwent Week: 200440

12/3,K/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2008 The Thomson Corporation. All rts. reserv.

0013997790 - Drawing available
WPI ACC NO: 2004-178974/200417
XRPX Acc No: N2004-142285
Integrated circuit of microprocessor, includes standard chip-level test access port controller that stores core select bits, each indicating whether corresponding core is selected for built-in self test (BIST) operation
Patent Assignee: PENDURKAR R Y (PEND-I); SUN M CROSYSTEMS INC (SUNM)
Inventor: PENDURKAR R Y
Patent Family (6 patents, 101 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
US 20040006729	A1	20040108	US 2002189870	A	20020703	200417	B
WO 2004005949	A1	20040115	WO 2003US21101	A	20030702	200417	E
AU 2003249712	A1	20040123	AU 2003249712	A	20030702	200459	E
GB 2404446	A	20050202	WO 2003US21101	A	20030702	200510	E
			GB 200425535	A	20041119		
TW 225199	B1	20041211	TW 2003118226	A	20030703	200535	E
TW 200405166	A	20040401	TW 2003118226	A	20030703	200568	E

Priority Applications (no., kind, date): US 2002189870 A 20020703

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20040006729	A1	EN	15	8	
WO 2004005949	A1	EN			

National Designated States, Original: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
Regional Designated States, Original: AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT RO SD SE SI SK SL SZ TR TZ UG ZM ZW

AU 2003249712	A1	EN	Based on OPI patent WO 2004005949
GB 2404446	A	EN	PCT Application WO 2003US21101 Based on OPI patent WO 2004005949
TW 225199	B1	ZH	
TW 200405166	A	ZH	

Integrated circuit of microprocessor, includes standard chip-level test access port controller that stores core select bits, each indicating whether corresponding core is selected for built-in self test (BIST) operation

Alerting Abstract ...elements, core-level master BIST (built-in self test) controller (304) and standard core-level **test access port (TAP) controller** (302), integrally coupled to **each** other. A standard chip-level **test access port controller** coupled to chip-level master BIST controller, has a core select **register** for storing core select **bits**, each indicating whether a corresponding core is selected for a BIST operation.

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstract:
...access port (TAP) controller, a chip-level master BIST controller, and a test pin interface. **Each** processor core includes **a** JTAG-compliant **TAP controller** and one **or more** BIST-enabled memory arrays. The chip TAP controller includes one or more user defined **registers**, including a core **select register** and a test **mode register**. The core select **register** stores a plurality **of** core select **bits** that select corresponding **processor** cores for BIST operations...

...access port (TAP) controller, a chip-level master BIST controller, and a test pin interface. Each processor core includes a JTAG-compliant TAP controller and one or more BIST-enabled memory arrays. The chip TAP controller includes one or more user-defined registers, including a core select register and a test mode register. The core select register stores a plurality of core select bits that select corresponding processor cores for BIST operations.

Claims:
...port (TAP) controller coupled to the core master BIST controller; a chip-level master BIST controller coupled to each of cores; anda standard chip-level test access port (TAP) controller coupled to the chip-level master BIST controller and having a core select register for storing a plurality of core select bits, each indicating whether a correspondin core is selected for a BIST operation. Basic Derwent Week: 200417

12/3,K/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0013960681 - Drawing available
WPI ACC NO: 2004-141344/200414
XRPX Acc No: N2004-112776
Microchip burn-in test design generates pseudorandom test vectors based on message indicating burn-in test stage of microchip, and shifting generated vectors one-by-one into internal scan chain of flip flop
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: GOLSHAN F
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 6675338 B1 20040106 US 2000635996 A 20000809 200414 B

Priority Applications (no., kind, date): US 2000635996 A 20000809

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 6675338 B1 EN 5 3

Original Publication Data by Authority
Argentina

Assignee name & address:
Claims:
...controller having a first input, a second input, and an output; a Linear Feedback Shift Register (LFSR) having an input and an output, said input of said LFSR coupled to said output of said TAP controller, wherein said LFSR further includes an XOR gate having five inputs and an output, an output on each of a last, second-to-last, third-to-last, twenty-second-to-last, and first...

12/3,K/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0013498290 - Drawing available
WPI ACC NO: 2003-590807/ 200356
XRAM Acc No: C2003-160458
XRPX Acc No: N2003-470339
Semiconductor integrated circuit for copier, has noise detectors to detect noise mixing corresponding to each boundary scan register cell and to output result through shift output terminal
Patent Assignee: KONICA CORP (KONS)
Inventor: TAKAGHI H; TAKAGI M
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update

JP 2003057306 A 20030226 JP 2001246156 A 20010814 200356 B

Priority Applications (no., kind, date): JP 2001246156 A 20010814

Patent Details
Number Kind Lan Pg Dwg Filing Notes
JP 2003057306 A JA 11 8

Alerting Abstract ...output shift terminal (114) for boundary scan test. A switching unit switches the signal from test access port controller (105) and stores each sampling clock which is higher than standard clock frequency in memory of each boundary scan register cell (110) based on which several noise detectors detect the noise mixing. A shift output...

Original Publication Data by Authority

Argentina...
...

12/3,K/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0012863738 - Drawing available
WPI ACC NO: 2002-722632/ **200278**
Related WPI Acc No: 2002-537842
XRPX Acc No: N2002-569835
Circuit nodes sequentially accessing method in IEEE 1149.4 compatible mixed signal circuit, involves shifting switch enabling logic value to next boundary module and monitoring or driving corresponding signal node
Patent Assignee: SUNTER S K (SUNT-I)
Inventor: SUNTER S K
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 20020099990 A1 20020725 US 2001768501 A 20010125 200278 B

Priority Applications (no., kind, date): US 2001768501 A 20010125

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 20020099990 A1 EN 20 13

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...in an IEEE 1149.4 compatible mixed-signal circuit having a test access port controller, a boundary scan register having a boundary module associated with each circuit node, analog busses for accessing the circuit nodes and connecting the analog bus pins...

...each boundary module, the boundary modules having analog switches for selectively accessing the busses, shift register elements and associated update latches for controlling the analog switches, the method comprising initializing the boundary modules with logic...
Claims:

12/3,K/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0012687108 - Drawing available
WPI ACC NO: 2002-537842/ **200257**
Related WPI Acc No: 2002-722632
XRPX Acc No: N2002-425884
Sequential circuit node accessing method for signal mixer circuit, involves

shifting switch-enabling logic value from one boundary module to next module after suppressing capture operation in each boundary module
Patent Assignee: LOGICVISION INC (LOGI-N)
Inventor: SUNTER S K
Patent Family (4 patents, 96 countries)
Patent Application
Number Kind Date Number Kind Date Update
WO 2002052289 A1 20020704 WO 2001CA1683 A 20011129 200257 B
CA 2329597 A1 20020622 CA 2329597 A 20001222 200257 E
US 6691269 B2 20040210 US 2001768501 A 20010125 200413 E
AU 2002221391 A1 20020708 AU 2002221391 A 20011129 200427 E

Priority Applications (no., kind, date): CA 2329597 A 20001222

Patent Details
Number Kind Lan Pg Dwg Filing Notes
WO 2002052289 A1 EN 37 13
National Designated States, Original: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Regional Designated States, Original: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW
CA 2329597 A1 EN
AU 2002221391 A1 EN Based on OPI patent WO 2002052289

Alerting Abstract ...and reduces the number of clock cycles required to access subsequent node by shifting the switch enabling bit from one BSR. Provides rapid access mode to facilitate rapid sequential access of the circuit...

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstract:
...in an IEEE 1149.4 compatible mixed-signal circuit having a test access port controller, a boundary scan register having a boundary module associated with each circuit node, analog busses for accessing the circuit nodes and connecting the analog bus pins...

...each boundary module, the boundary modules having analog switches for selectively accessing the busses, shift register elements and associated update latches for controlling the analog switches, the method comprising initializing the boundary modules with logic...
Claims:
...IEEE 1149.4 compatible mixed-signal circuit having a test access port controller having a plurality of states including ShiftDR, UpdateDR and CaptureDR, a boundary scan register having a boundary module associated with each said...
Basic Derwent Week: 200257

12/3,K/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2008 The Thomson Corporation. All rts. reserv.

0012667329 - Drawing available
WPI ACC NO: 2002-517344/ 200255
Related WPI Acc No: 2002-487999; 2002-705204
XRPX Acc No: N2002-409297
Snoopy test access port architecture has controller which regulates switch to disconnect first port from second port when snoopy instruction register stores predetermined wake-up instruction
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: BHATTACHARYA D
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 6381717 B1 20020430 US 199882992 P 19980424 200255 B

Priority Applications (no., kind, date): US 1999882992 P 19980424; US 1999298801 A 19990423

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 6381717 B1 EN 26 18 Related to Provisional US 199882992

Alerting Abstract ...existing taped core without requiring any modification to the existing core. Eliminates necessity for a **second test access port controller** contained within the test access port linking module. Enables simplification of the design and test...

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...of the electronic circuit. An internal state in the test access port controller, such as **bits** in a data register, controls the **switch** state of the programmable switch. When an embedded core circuit is connected for test, the...
Claims:
...port operating in accordance with said predetermined set of a plurality of test states;a **test access port controller** connected to said first test access port, said test access port controller including a switch ...

...port to said second test access port of one of said plurality of testable embedded **core circuits**, **said test access port controller** operating in a one of a **plurality** of **snoopy states corresponding to** said test state of said second test access port, said test access port including a snoopy instruction **register** loadable from said test data input line when said test access **port** controller is in a snoopy state corresponding to an instruction input state of one of...

...core circuits, said test access port controller controlling said programmable switch to disconnect said first **test access port from** said second test access port of **all** said at least one testable embedded core circuit when said snoopy instruction **register** stores a predetermined wake-up instruction. Basic Derwent Week: **200255**

12/3,K/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0012264111 - Drawing available
WPI ACC NO: 2002-204296/ **200226**
XRPX Acc No: N2002-155343
Integrated circuit tester for IC chips having multiple cores and associated Test Link Modules (TLM) where each core has an internal TM with a register for storing instructions and a bit for storing an instruction passing indication signal
Patent Assignee: PHILIPS SEMICONDUCTORS INC (PHIG)
Inventor: ADUSUMILLI S; CASSETTI D; STEELE J
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 6311302 B1 20011030 US 1999283648 A 19990401 200226 B

Priority Applications (no., kind, date): US 1999283648 A 19990401

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 6311302 B1 EN 7 2

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...specification and without requiring more scan chains per TAPprimeed core. One particular example embodiment includes **each** of the designprimes multiple cores including multiple **test - access port (TAP) controllers**, and including an internal TLMhaving a TLM **register** adapted to store a decodable instruction and a supplemental storage circuit adapted to store a...
Claims:
...access pins for selecting functions internal to the IC, comprising:multiple cores within the IC, **each** of the multiple **cores** including multiple **test - access port (TAP) controllers** and including an internal TLM, wherein the TLMincludes a storage unit having a TLM **register** adapted to store a decodable instruction and a supplemental storage circuit adapted to store a coded signal; anda...

...coupled with a common interface and with each of the multiple cores via the TLM **register** and the supplemental storage circuit, wherein the chip-level TLM and the multiple cores are...
Basic Derwent Week: **200226**

12/3,K/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0010627403 - Drawing available
WPI ACC NO: 2001-233950/ **200124**
XRPX Acc No: N2001-167179
Boundary scan compliant component couples each boundary scan register cell to unclocked input buffer, if instruction register is loaded with one of IEEE 1149.1 defined test instruction
Patent Assignee: COMPAQ COMPUTER CORP (COPQ)
Inventor: BHAVSAR D K; BIROL L
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 6163864 A 20001219 US 199895149 A 19980610 200124 B

Priority Applications (no., kind, date): US 199895149 A 19980610

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 6163864 A EN 12 5

Original Publication Data by Authority
Argentina

Assignee name & address:
Original Abstracts:
...is a clocked and an unclocked input buffer. Coupled to the TAP is an instruction **register** for receiving Standard defined and other test instructions provided by the external circuitry at the...

...associated with a different one of the input pins and connected to the output of **each** input buffer coupled thereto, and a **TAP controller** for generating control signals to capture and shift data through the boundary scan cells in response to test instructions received by the instruction **register**. Compliance control circuitry, responsive to the instruction **register** and the **TAP controller**, operates to couple **each** BSR cell to the second input buffer when the instruction **register** has been loaded with a Standard defined instruction. When the instruction **register** has been loaded with an instruction corresponding to an input threshold voltage test of the...
Claims:
...being responsive to the forwarded clock; input an instruction register coupled to the TAP, the **instruction register** for receiving IEEE 1149.1 **defined** and other test instructions provided by the external test circuitry at the TAP; a boundary scan **register** coupled to the TAP, the boundary scan **register** including boundary scan cells associated with each of the input pins and connected to the output of **each** input buffer coupled thereto; a **TAP controller** for generating control signals to

capture data from **outputs of** the input buffers into the boundary scan cells to which the input buffers are connected...

...data through the boundary scan cells in response to test instructions received by the instruction **register**; and compliance control circuitry, responsive to the instruction **register and** the TAP controller, for selectively coupling outputs of the first **and** second input **buffers connected** to **each** data input pin for capture by the BSR cell with which the input pin is...

...compliance control circuitry coupling each BSR cell to the second input buffer when the instruction **register** has been loaded with one of the IEEE 1149.1 defined **test** instructions and coupling the BSR cell to the first input buffer when the instruction register...
Basic Derwent Week: **200124**

12/3,K/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0009446042 - Drawing available
WPI ACC NO: 1999-385103/ **199932**
XRPX Acc No: N1999-288438
Boundary scan tester for integrated circuits
Patent Assignee: ATMEL CORP (ATME-N)
Inventor: BERGER N; FAHEY; FAHEY J; GONGWER G S; JINGLUN T; RAMAMURTHY S; SAIKI W J; TAM J
Patent Family (13 patents, 26 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
WO 1999024841	A1	19990520	WO 1998US23420	A	19981103	199932	B
US 6032279	A	20000229	US 1997965919	A	19971107	200018	E
NO 200002268	A	20000706	WO 1998US23420	A	19981103	200044	E
			NO 20002268	A	20000428		
EP 1036338	A1	20000920	EP 1998956523	A	19981103	200047	E
			WO 1998US23420	A	19981103		
TW 411393	A	20001111	TW 1998118562	A	19981107	200121	E
CN 1278332	A	20001227	CN 1998810850	A	19981103	200123	E
KR 2001040269	A	20010515	KR 2000704881	A	20000504	200167	E
JP 2001523005	W	20011120	WO 1998US23420	A	19981103	200204	E
			JP 2000519793	A	19981103		
EP 1036338	B1	20041020	EP 1998956523	A	19981103	200469	E
			WO 1998US23420	A	19981103		
DE 69827159	E	20041125	DE 69827159	A	19981103	200477	E
			EP 1998956523	A	19981103		
			WO 1998US23420	A	19981103		
NO 317781	B1	20041213	WO 1998US23420	A	19981103	200482	E
			NO 20002268	A	20000428		
DE 69827159	T2	20051117	DE 69827159	A	19981103	200576	E
			EP 1998956523	A	19981103		
			WO 1998US23420	A	19981103		
CN 1176383	C	20041117	CN 1998810850	A	19981103	200617	E

Priority Applications (no., kind, date): US 1997965919 A 19971107

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 1999024841	A1	EN	20	3	
National Designated States,Original:			CA CN JP KR NO SG		
Regional Designated States,Original:			AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE		
NO 200002268	A	NO			PCT Application WO 1998US23420
EP 1036338	A1	EN			PCT Application WO 1998US23420
					Based on CPI patent WO 1999024841
Regional Designated States,Original:			DE FR GB IT NL		
TW 411393	A	ZH			
JP 2001523005	W	JA	22		PCT Application WO 1998US23420
					Based on CPI patent WO 1999024841
EP 1036338	B1	EN			PCT Application WO 1998US23420
					Based on CPI patent WO 1999024841
Regional Designated States,Original:			DE FR GB IT NL		

DE 69827159	E	DE	Application EP 1998956523 PCT Application WO 1998US23420 Based on CPI patent EP 1036338 Based on CPI patent WO 1999024841
NO 317781	B1	NO	PCT Application WO 1998US23420 Previously issued patent NO 200002268
DE 69827159	T2	DE	Application EP 1998956523 PCT Application WO 1998US23420 Based on CPI patent EP 1036338 Based on CPI patent WO 1999024841

Original Publication Data by Authority
Argentina

Assignee name & address:
Claims:
...port controller connected to dedicated Boundary Scan pins including TMS and TCK pins, an instruction **register** communicating with the test access port controller and connected to dedicated Boundary Scan pins including...

...a boundary register, a bypass register, a plurality of test data registers and an address **register** all **connected** in **parallel** **between** the TDI and TDO pins. **all** of said **registers** communicating with the instruction **register**, said **address** **register** being loaded with an address that points to a specific one of the test **registers**, a software instruction set adapted for decoding **by** the instruction **register**, said instruction set having first **instructions** dependent on an **address** of a target test data register and second instructions which are independent of addresses and...
Basic Derwent Week: **199932**

12/3,K/14 **(Item 14 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
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0009205656 - Drawing available
WPI ACC NO: 1999-130669/ **199911**
XRPX Acc No: N1999-095101
Hierarchically managed testable module for boundary scan testing - has multiple slave components each one having slave component boundary scan register coupled serially to form boundary scan chain whose input and output are coupled to master component
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: DIETRICH B L; HANDLY P R; YOCKEY R F
Patent Family (1 patents, 1 countries)
Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 5862152	A	19990119	US 1995558122	A	19951113	199911 B

Priority Applications (no., kind, date): US 1995558122 A 19951113

Patent Details
Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5862152	A	EN	10	3	

Alerting Abstract ...20) has a test access port (TAP) controller which controls a master component boundary scan **register**. Multiple slave components (22) have respective slave component boundary scan **register** which is controlled by **TAP** **controller** of master component. **All** the slave component boundary scan **registers** are coupled serially to form a boundary scan chain having an input and output both...

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...component having a test-access-port (TAP) controller and having a master component boundary-scan **register** coupled to and **controlled** by said TAP

controller; a slave component having a slave component boundary-scan register coupled to and controlled by said TAP controller of said master component; said slave component is one of a plurality of slave components each having a boundary-scan register coupled to and controlled by said TAP controller of said master component and; each said slave component boundary-scan register of said plurality of slave components is serially coupled together into a boundary-scan chain having an input coupled to said master component and an...
Basic Derwent Week: 199911

12/3,K/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2008 The Thomson Corporation. All rts. reserv.

0005480452 - Drawing available
WPI ACC NO: 1991-082104/ 199112
XRPX Acc No: N1991-063430
Dynamically reconfigurable signal processor - uses tap sections which can be reconfigured with coefficients and transfer paths on each cycle
Patent Assignee: PHILIPS ELECTRONICS NV (PHIG); PHILIPS GLOEILAMPENFAB NV (PHIG)
Inventor: BASILE C; JOHNSON B; JOHNSON B C; LEONARD J; MIRON A; TERMAN C; TERMAN C J; WESTE N; WESTE N H E
Patent Family (6 patents, 5 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
EP 417861	A	19910320	EP 1990202406	A	19900910	199112	B
US 5034907	A	19910723	US 1989406203	A	19890912	199132	E
			US 1990614043	A	19901109		
JP 3174813	A	19910730	JP 1990242281	A	19900912	199136	E
EP 417861	A3	19920916	EP 1990202406	A	19900910	199339	E
EP 417861	B1	19980610	EP 1990202406	A	19900910	199827	E
DE 69032385	E	19980716	DE 69032385	A	19900910	199834	E
			EP 1990202406	A	19900910		

Priority Applications (no., kind, date): US 1990614043 A 19901109; US 1989406203 A 19890912

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 417861	A	EN			
Regional Designated States, Original: DE FR GB					
EP 417861	A3	EN			
EP 417861	B1	EN			
Regional Designated States, Original: DE FR GB					
DE 69032385	E	DE			Application EP 1990202406
					Based on CPI patent EP 417861

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...it, and a third data path (3a-3h) connected to the tap above it. A controller (16) contains memory to store both multi-bit coefficients and control words available at he taps via a bus (225) at each cycle. The control words reconfigure...
...

14/3,K/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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04272964 **Image available**
SEMICONDUCTOR INTEGRATED CIRCUIT

PUB. NO.: 05-264664 [JP 5264664 A]
PUBLISHED: October 12, 1993 (19931012)
INVENTOR(s): ITO TAKAYUKI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-058715 [JP 9258715]
FILED: March 17, 1992 (19920317)
JOURNAL: Section: P, Section No. 1677, Vol. 18, No. 31, Pg. 90, January 18, 1994 (19940118)

ABSTRACT

... test data resister part 1 consisting of a plurality of resisters to be tested; a **TAP controller** 2 for supplying a clock signal to **each** resister of the test data resister part 1: an instruction resister 3 for temporarily storing...

... instruction decoder 4 for analyzing the command stored in the instruction resister 3; and a **switching** means 1 for selectively **switching** whether the clock signal from the **TAP controller** 2 is outputted to **each** resister of the test data resister part 1. The **switching** means 11 supplies the clock signal only to the resister which is a test target...

14/3,K/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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00940421 **Image available**
TAP SWITCHING CONTROLLER

PUB. NO.: 57-090721 [JP 57090721 A]
PUBLISHED: June 05, 1982 (19820605)
INVENTOR(s): YOSHIDA KATSUYA
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-166757 [JP 80166757]
FILED: November 28, 1980 (19801128)
JOURNAL: Section: P, Section No. 141, Vol. 06, No. 175, Pg. 44, September 09, 1982 (19820909)

ABSTRACT

PURPOSE: To increase the lifetime of a **tap switching controller**, by applying the voltage reference value to **both** a tap **switching** device and a voltage controller from a setter and accordingly not only simplifying the control...

14/3,K/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0014505872 - Drawing available
WPI ACC NO: 2004-687791/200467
XRPX Acc No: N2004-544696
Tap multiplexer controller for use in wide area network e.g. asynchronous transfer mode network, has processor executing computer instructions defining logic to initiate fixed length window of time on detection of error
Patent Assignee: NORTEL NETWORKS LTD (NELE)
Inventor: HUNTER V; REDDY S; SENEVIRATHNE T
Patent Family (1 patents, 1 countries)
Patent Application

Number	Kind	Date	Number	Kind	Date	Update	
US 6798740	B1	20040928	US 2000524093	A	20000313	200467	B

Priority Applications (no., kind, date): US 2000524093 A 20000313

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 6798740	B1	EN	15	7	

Original Publication Data by Authority

Argentina

Assignee name & address:

Original Abstracts:

A method and apparatus selecting between primary **switching** fabric in an **asynchronous** transfer mode (ATM) network includes a **Tap** Mux **controller** that **monitors** the **signals** being transmitted to **each** of four fabric **access** devices. As each of the fabric **access** devices receives nine communication lines, the **Tap** Mux **controller** monitors a total for 36 communication lines on the primary **switching** fabric. Because the **switching** fabric is completely **redundant**, however, the Tap Mux controller also monitors a total of 36 communication lines on the protection **switching** fabric. The Tap **Mux** controller, therefore, **includes** logic that defines 72 state machines that **each** monitor one of the 72 lines. Each state machine, in the described embodiment, initiates a defined length time window and counts errors therein. Protection path **switching** occurs, for example, **only** when 10 errors occur on any one of the 36 primary **switching** fabric lines being **received** by four fabric access devices therein within a 100 millisecond window initiated at the detection...

Claims:

14/3,K/4 (Item 2 from file: 350)

0014442986 - Drawing available

WPI ACC NO: 2004-633638/200461

Related WPI Acc No: 2005-795246; 2006-077823

XRPX Acc No: N2004-500816

Optical switch in cable television system, has photodiode connected to one of the two tap couplers in each path, and optical fiber connected between other couplers to couple optical signal in backup path, to primary path

Patent Assignee: GEN INSTR CORP (GENN); JASTI C S (JAST-I)

Inventor: JASTI C S

Patent Family (3 patents, 106 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
US 20040156579	A1	20040812	US 2003364825	A	20030211	200461	B
WO 2004072690	A2	20040826	WO 2004US3538	A	20040206	200461	E
US 6944362	B2	20050913	US 2003364825	A	20030211	200560	E

Priority Applications (no., kind, date): US 2003364825 A 20030211

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20040156579	A1	EN	5	2	
WO 2004072690	A2	EN			

National Designated States, Original: AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NA NI NO NZ OM PG PH PL PT RO RU SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW

Regional Designated States, Original: AT BE BG BW CH CY CZ DE DK EA EE ES FI FR GB GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT RO SD SE SI SK SL SZ TR TZ UG ZM ZW

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...the secondary path is coupled onto the primary path; anda controller electrically coupled to **each** of the optical **switches**, **said controller** being configured so that when **each** of the **switching** elements are in said second state and the first photodetector in each of the optical **switches** detects an optical signal, said controller returns the **switching** elements **to** said first state.

14/3,K/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0012846700 - Drawing available
WPI ACC NO: 2002-705204/200276
Related WPI Acc No: 2002-487999; 2002-517344
XRPX Acc No: N2002-555838
Electronic circuit has programmable switch that connects test access ports of embedded core circuits and test access port controller for controlling test of core circuits based on internal test state of controller
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: BHATTACHARYA D
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 6425100 B1 20020723 US 199882992 P 19980424 200276 B
US 1999298138 A 19990423

Priority Applications (no., kind, date): US 199882992 P 19980424; US 1999298138 A 19990423

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 6425100 B1 EN 27 18 Related to Provisional US 199882992
Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...set of input and output lines of said first test access port; anda programmable **switch** coupled to said first test access port, said second **test** access port of each of said plurality of testable embedded core circuit and **said test access port controller**, said programmable **switch** selectively connecting said first test access port to said **second** test access port of one of said plurality of testable embedded core circuit for controlling...

14/3,K/6 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0012638923 - Drawing available
WPI ACC NO: 2002-487999/200252
Related WPI Acc No: 2002-517344; 2002-705204
XRPX Acc No: N2002-385619
Electronic circuit with hierarchical test access port architecture, has programmable switch that selectively connects to test access ports for controlling core circuit testing based test state
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: BHATTACHARYA D
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 6378090 B1 20020423 US 199882992 P 19980424 200252 B
US 1999298018 A 19990423

Priority Applications (no., kind, date): US 199882992 P 19980424; US 1999298018 A 19990423

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 6378090 B1 EN 27 18 Related to Provisional US 199882992
Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...of input and output lines of said second test access port, anda first programmable **switch** coupled to said second test access port, said third test access port of **each** of said at least one second testable embedded core circuit and said first **test access port controller**, said first programmable **switch** selectively connecting said second test access port to said third test access port **of** one of said at least one second testable embedded core circuit for controlling test of...

...of said first test access port controller;at least one third testable embedded core circuit **each** having **a fourth test access port** including said predetermined set of input and output lines adapted for controlling electronic test of...

...of input and output lines of said first test access port; anda second programmable **switch** coupled to said first test access port, said second test access port and said fourth test access port of **each** of said at least one third testable embedded core circuit and said first **test access port controller, said** second **programmable switch** selectively connecting said first test access port to said second test access port or to a selected one of **said** fourth test access port of one of said at least one third testable embedded core...

14/3,K/7 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0010463813 - Drawing available
WPI ACC NO: 2001-063497/200108
XRPX Acc No: N2001-047810
Electrical power ring device for military vehicle has power ring bus divided into ring line segments coupled via power ring controllers at each energy supply or tap-off node
Patent Assignee: MAK SYSTEM GMBH (MAKS-N); RHEINMETALL LANDSYSTEME GMBH (RHEM)
Inventor: HERNEKAMP C; JOEHNKE V
Patent Family (6 patents, 25 countries)
Patent Application
Number Kind Date Number Kind Date Update
EP 1044851 A2 20001018 EP 2000101548 A 20000127 200108 B
DE 19916452 A1 20001026 DE 19916452 A 19990412 200108 E
DE 19916452 C2 20011025 DE 19916452 A 19990412 200164 E
US 6552443 B1 20030422 US 2000548335 A 20000412 200330 E
EP 1044851 B1 20040915 EP 2000101548 A 20000127 200460 E
DE 50007723 G 20041021 DE 50007723 A 20000127 200469 E
EP 2000101548 A 20000127

Priority Applications (no., kind, date): DE 19916452 A 19990412; EP 2000101548 A 20000127

Patent Details
Number Kind Lan Pg Dwg Filing Notes
EP 1044851 A2 DE 6 3
Regional Designated States,Original: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
EP 1044851 B1 DE
Regional Designated States,Original: DE FR GB NL SE
DE 50007723 G DE Application EP 2000101548
Based on OPI patent EP 1044851

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...right of one of the tap controllers can be disconnected or connected via the controlled switches (3), and by means of which the electrical appliance can be disconnected or connected as...
...1), so that the tap and the feed point on the ring line (9) are each physically combined with the tap controller (1...

...en tant que consommateurs au cable annulaire (9) et en des points d'alimentation (10) sur le cable annulaire (9) pour l'alimentation (10) en energie electrique ainsi qu'une connexion...

...superpose servant a controler et a commander le cable annulaire (9), caracterise en ce que le controleur (1) est un controleur de captage qui presente un raccordement (5) et un nodule de commande (2) ainsi qu'un...
?

19/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0016192072 - Drawing available
WPI ACC NO: 2006-723713/200675
XRPX Acc No: N2006-568556
Joint test action group test access port controller nesting method, involves selecting available bit from selectable bit register of host joint test action group test access port controller, where register has available bits
Patent Assignee: XILINX INC (XILI-N)
Inventor: SCHULTZ D P
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 7111217 B1 20060919 US 200286129 A 20020228 200675 B

Priority Applications (no., kind, date): US 200286129 A 20020228

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 7111217 B1 EN 12 3

...action group test access port controller nesting method, involves selecting available bit from selectable bit register of host joint test action group test access port controller, where register has available bits

Alerting Abstract ...NOVELTY - The method involves selecting an internal protocol (IP) core joint test action group test access port (JTAG TAP) controller to be coupled in series with a host JTAG TAP controller. An available bit is selected from a selectable bit register of the controller, where the bit register has available bits. An apparent length of an instruction register of the controller is extended by using the available bit from the selectable bit register.... a method for ensuring an information register length for nested joint test action group test access port controllers for IP cores; a system for flexibly accessing nested JTAG TAP controllers for IP cores...

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
A flexible architecture for nesting joint test action group (JTAG) test access port (TAP) controllers for FPGA-based embedded system-on-chip (SoC) is provided. Advantageously, a programmable approach permits bits in a selectable bit register (302) to be selected based on the number of JTAG TAPs that will be utilized. The selected bits can be used to vary the apparent length of an instruction register (302). Importantly, the flexible architecture permits access to any combination of a plurality of JTAG TAP controllers in the FPGA-based embedded SoC without the need to rewire any I/O pins...
Claims: Basic Derwent Week: 200675

19/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0015409967 - Drawing available
WPI ACC NO: 2005-755891/200577
Related WPI Acc No: 2002-077143; 2002-084478; 2002-473296; 2004-764313; 2005-045939; 2006-063534; 2006-625648; 2006-645723; 2007-857021; 2008-D49252; 2008-D49420
XRPX Acc No: N2005-623609
Integrated circuit, has join test action group circuit with data registers that are designed to perform functions which are not performed by

pre-existing data registers, where circuit has test access port controller
Patent Assignee: ALTERA CORP (ALTE-N)
Inventor: DRAPER A M
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 6961884 B1 20051101 US 2000211094 P 20000612 200577 B
US 2001880749 A 20010612

Priority Applications (no., kind, date): US 2000211094 P 20000612; US 2001880749 A 20010612

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 6961884 B1 EN 21 16 Related to Provisional US 2000211094

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...wherein the first JTAG circuit comprises a first TAP controller coupled to a first instruction **register** and a first plurality of data **registers** ; andan embedded logic portion comprising a processor and a second JTAG circuit coupled to the first JTAG circuit and to the processor, wherein the second JTAG circuit comprises a **second TAP controller** coupled to a second instruction **register** and a second plurality of data **registers** , and at least some of the second plurality of data **registers** in the second JTAG circuit are designed to perform functions that are not performed by the first plurality of data **registers.**> Basic Derwent Week: 200577

19/3,K/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2008 The Thomson Corporation. All rts. reserv.

0015146448 - Drawing available
WPI ACC NO: 2005-496022/200550
XRPX Acc No: N2005-404509
Driver integrated circuit for LED printhead, has circuitry with control register for enabling token bypass function so that circuitry bypasses received data from register in response to token received from token input
Patent Assignee: CHARA S E (CHAR-I); REILLY D P (REIL-I); EASTMAN KODAK CO (EAST)
Inventor: CHARA S E; REILLY D P
Patent Family (2 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 20050140773 A1 20050630 US 2003532288 P 20031223 200550 B
US 200412977 A 20041215
US 7236183 B2 20070626 US 200412977 A 20041215 200742 E

Priority Applications (no., kind, date): US 2003532288 P 20031223; US 200412977 A 20041215

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 20050140773 A1 EN 7 3 Related to Provisional US 2003532288

Alerting Abstract ...NOVELTY - The circuit has a circuitry (100) with a joint test action group control **register** (103) that enables a token bypass function so that the circuitry bypasses received data from the **register** in response to token received from a token input. The circuitry has a joint test action **group tap controller** (102) accessing the **register** . A data bus couples the data to the **registers** . A clock input is coupled to the **register** and a flip-flop.

Original Publication Data by Authority

ArgentinaBasic Derwent Week: 200550

19/3,K/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0010545956 - Drawing available
WPI ACC NO: 2001-149172/ **200116**
XRPX Acc No: N2001-109480
Integrated circuit comprises serial data input and output pins, on-chip functional circuitry and test logic, test access port controller and data adapter
Patent Assignee: STMICROELECTRONICS LTD (SGSA)
Inventor: WARREN R
Patent Family (4 patents, 25 countries)
Patent Application
Number Kind Date Number Kind Date Update
EP 1041390 A1 20001004 EP 2000301289 A 20000218 200116 B
US 6526535 B1 20030225 US 2000507829 A 20000222 200323 E
EP 1041390 B1 20050413 EP 2000301289 A 20000218 200525 E
DE 60019363 E 20050519 DE 60019363 A 20000218 200535 E
EP 2000301289 A 20000218

Priority Applications (no., kind, date): GB 19997254 A 19990329; EP 2000301289 A 20000218

Patent Details
Number Kind Lan Pg Dwg Filing Notes
EP 1041390 A1 EN 29 11
Regional Designated States, Original: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
EP 1041390 B1 EN
Regional Designated States, Original: DE FR GB IT
DE 60019363 E DE Application EP 2000301289
Based on CPI patent EP 1041390

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...which is connectable to the input and output pins via the test access port controller in a **second mode** of operation, wherein the data adaptor comprises a first interface for communicating data in the form of serial **bits** to and from **said** test access port controller under the control of a first clock signal and a second...
Claims:
...connectable to the input and output pins via the test access port controller in a **second** mode of operation, **wherein the data adaptor** comprises a first interface for communicating data in the form of serial **bits** to and from said test access port controller under **the** control of a first clock signal and a second interface for communicating data in the...
Basic Derwent Week: **200116**

19/3,K/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2008 The Thomson Corporation. All rts. reserv.

0009852493 - Drawing available
WPI ACC NO: 2000-146500/ **200013**
XRPX Acc No: N2000-108451
Automatic extraction and compliance checking method of boundary scan circuit
Patent Assignee: SYNOPSYS INC (SYNO-N)
Inventor: BEAUSANG J; SINGH H
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 6012155 A 20000104 US 1997961389 A 19971030 200013 B

Priority Applications (no., kind, date): US 1997961389 A 19971030

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 6012155 A EN 47 26

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...access port (TAP) controller design within said netlist; traversing a plurality of states of said **TAP controller** to verify compliance with a set of known states; controlling said TAP controller to extract shift cells of an instruction **register**; extracting and verifying a bypass **register** of said netlist; extracting cells of a boundary scan **register** of said netlist; classifying cells of said boundary scan **register** as an input, output or control cells; extracting a set of frontier pins associated with decode logic...
Basic Derwent Week: **200013**

19/3,K/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2008 The Thomson Corporation. All rts. reserv.

0009182745 - Drawing available
WPI ACC NO: 1999-106615/ **199910**
XRPX Acc No: N1999-077007
Interface to transfer serial test data from test access port in different clock domain - has circuits to derive synchronised pulse and hold signals, to derive synchronised shift signal and to retime serial data according to these signals
Patent Assignee: LOGICVISION INC (LOGI-N)
Inventor: COTE J; NADEAU-DOSTIE B
Patent Family (3 patents, 2 countries)
Patent Application
Number Kind Date Number Kind Date Update
CA 2233493 A 19980928 CA 2233493 A 19980327 199910 B
US 5900753 A 19990504 US 1997825446 A 19970328 199925 E
CA 2233493 C 20000530 CA 2233493 A 19980327 200040 E

Priority Applications (no., kind, date): US 1997825446 A 19970328

Patent Details
Number Kind Lan Pg Dwg Filing Notes
CA 2233493 A EN 38 10
CA 2233493 C EN

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
An interface allowing to transfer serial test data from a **Test Access Port (TAP) to controllers located in several clock** domains is described. The clock frequencies can be different from each other and do not...

...to work reliably as long as the clock frequencies used for the test controllers and **registers** is 3 times higher than the one of the TAP used to source the serial...
Claims: Basic Derwent Week: **199910**

19/3,K/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2008 The Thomson Corporation. All rts. reserv.

0008967387 - Drawing available
WPI ACC NO: 1998-520538/ **199844**

Related WPI Acc No: 1997-350518
XRPX Acc No: N1998-406554
Boundary scan master operating method for testing electronic circuits - involves identifying time at which EXTEST instruction is loaded in instruction register of IC and TAP controller attains EXIT1-DR state
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: CHAMPLIN C R
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
US 5809036	A	19980915	US 1993158345	A	19931129	199844	B

Priority Applications (no., kind, date): US 1993158345 A 19931129

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5809036	A	EN	13	6	

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...TMS) signal which controls Boundary-Scan testing of an integrated circuit (IC) having an instruction **register** and a test access port (TAP) controller **for** operating in a **plurality of states**, **including** an EXIT1-DR state; andwherein said determining step comprises a step of identifying when said EXTEST instruction is loaded in said instruction **register** of said IC and said TAP controller has entered **said** EXIT1-DR state. Basic Derwent Week: **199844**

19/3,K/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2008 The Thomson Corporation. All rts. reserv.

0008866652 - Drawing available
WPI ACC NO: 1998-414259/ **199835**
XRPX Acc No: N1998-322374
Fault isolation system for microprocessor-based integrated circuit - has multiple shift registers globally controlled but individually driven by local clock phases during functional block under observation
Patent Assignee: ROCKWELL INT CORP (ROCW)
Inventor: BORDEN C E; MARTINEZ M A; TAYLOR A D
Patent Family (4 patents, 20 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
WO 1998032025	A1	19980723	WO 1998US819	A	19980116	199835	B
US 5790561	A	19980804	US 1997785068	A	19970117	199838	E
EP 943100	A1	19990922	EP 1998903520	A	19980116	199943	E
			WO 1998US819	A	19980116		
JP 2000514194	W	20001024	JP 1998534544	A	19980116	200058	E
			WO 1998US819	A	19980116		

Priority Applications (no., kind, date): US 1997785068 A 19970117

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 1998032025	A1	EN	26	9	
National Designated States,Original:		JP			
Regional Designated States,Original:		AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE			
EP 943100	A1	EN			PCT Application WO 1998US819 Based on CPI patent WO 1998032025
Regional Designated States,Original:		AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE			
JP 2000514194	W	JA	27		PCT Application WO 1998US819 Based on CPI patent WO 1998032025

Alerting Abstract ...in accordance with a control signal received from the global controller, and clocks the shift **register** in time coordination

with the local clock signal without direct connection to the external test ...

...a special user command via a test data input of a standard Joint Test Action Group (JTAG) tap controller (20), the global controller decoding the special user command...

Original Publication Data by Authority

Argentina Basic Derwent Week: 199835

19/3,K/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2008 The Thomson Corporation. All rts. reserv.

0008669083 - Drawing available
WPI ACC NO: 1998-207563/ 199818
XRPX Acc No: N1998-164798
Solid state voltage regulator for on-load transformer tap changer - has controller that senses regulator input and output voltages and generates gating signals to connect switch that results in greatest voltage compensation
Patent Assignee: ABB POWER T & D CO INC (ALLM)
Inventor: BAPAT V N
Patent Family (3 patents, 76 countries)
Patent Application
Number Kind Date Number Kind Date Update
WO 1998011476 A1 19980319 WO 1997US15028 A 19970826 199818 B
AU 199740918 A 19980402 AU 199740918 A 19970826 199833 E
US 5786684 A 19980728 US 1996710318 A 19960916 199837 E

Priority Applications (no., kind, date): US 1996710318 A 19960916

Patent Details
Number Kind Lan Pg Dwg Filing Notes
WO 1998011476 A1 EN 14 3
National Designated States, Original: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
Regional Designated States, Original: AT BE CH DE DK EA ES FI FR GB GH GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
AU 199740918 A EN Based on OPI patent WO 1998011476

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...capability of being turned on in response to a gate signal. A second solid state switch is connected between the regulator output and a second tap. The second switch has the capability of being turned on and turned off in response to gating signals. The output voltage resulting from the second tap is greater than the first tap. A controller, connected to the input, the output, the first switch and the second switch, senses the voltage present at the regulator input and output and generates gating signals in response to the sensed voltage. The voltage regulator may include several switches similar in construction and operation to the first switch. In such a regulator, the second switch is connected to the tap which results in...

...capability of being turned on in response to a gate signal. A second solid state switch (36) is connected between the regulator output (14) and a second tap (22). The second switch (36) has the capability of being turned on and turned off in response to gating signals. The output voltage resulting from the second tap (22) is greater than the first tap (20). A controller (16) connected to the input (12), the output (14), the first switch (34) and the second switch (36) senses the voltage present at the regulator input (12) and output (14) and generates gating signals in response to the sensed voltage. The voltage

regulator (10) may include several **switches** (38-46) similar in construction and operation to the first switch (34). In such a...

15/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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01779856
CONNECTING MULTIPLE TEST ACCESS PORT CONTROLLERS THROUGH A SINGLE TEST ACCESS PORT
VERBINDUNG MEHRERER TESTZUGRIFFSPORTSTEUERUNGSVORRICHTUNGEN DURCH EIN EINZELTESTZUGRIFFSPORT
SYSTEME DE CONNEXION DE CONTROLEUR DE POINTS D'ACCES MULTIPLES D'ESSAI PAR L'INTERMEDIAIRE D'UN SEUL POINT D'ACCES
PATENT ASSIGNEE:
  Koninklijke Philips Electronics N.V., (200769), Groenewoudseweg 1, 5621 BA Eindhoven, (NL), (Proprietor designated states: all)
INVENTOR:
  STEINBUSCH, Otto, 1109 McKay Drive, MS-41SJ, San Jose, CA 95131, (US)
LEGAL REPRESENTATIVE:
  Eveleld, Koop Jan (135781), Philips Intellectual Property & Standards, P.O. Box 220, 5600 AE Eindhoven, (NL)
PATENT (CC, No, Kind, Date): EP 1579229 A1 050928 (Basic)
                             EP 1579229 B1 061122
                             WO 2004057357 040708
APPLICATION (CC, No, Date): EP 2003780425 031215; WO 2003IB5950 031215
PRIORITY (CC, No, Date): US 435395 P 021220
DESIGNATED STATES: AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES; FI; FR; GB; GR; HU; IE; IT; LI; LU; MC; NL; PT; RO; SE; SI; SK; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK
INTERNATIONAL PATENT CLASS (V7): G01R-031/3185
INTERNATIONAL CLASSIFICATION (V8 + ATTRIBUTES):
IPC + Level Value Position Status Version Action Source Office:
  G01R-0031/3185 A I F B 20060101 20040715 H EP
NOTE:
  No A-document published by EPO
LANGUAGE (Publication, Procedural, Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
      CLAIMS B (English) 200647 567
      CLAIMS B (German) 200647 508
      CLAIMS B (French) 200647 652
      SPEC B (English) 200647 3937
Total word count - document A 0
Total word count - document B 5664
Total word count - documents A + B 5664

...SPECIFICATION in a product design.
  US patent application US6311602 discloses an integrated circuit (IC) having a **plurality** of **TAP controllers**. To provide access to individual TAP controllers via the external test data in (TDI) and...

...data out (TDO) pins, the IC further comprises a chip-level TAP linking module (TLM). **Each TAP controller** is extended with an extension bit that is monitored by the chip-level TLM. As soon as a TAP controller is informed that access has to be transferred to **another TAP controller**, it sets its extension bit, thus signalling the chip-level TLM to expect the reception...

...single integrated circuit.
  Briefly, embodiments of the present invention provide circuits and methods for accessing **multiple** test access port (TAP) **controllers** on a single chip, which is important for compliance with the IEEE 1149.1 Standard...

...port to an outside observer. By adding a single bit to a data register of **each** of a **plurality** of **TAP controllers** along with straightforward combinational glue logic, the **plurality** of **TAP controllers** can be accessed without the need for additional chip pins, and without the need for **additional TAP controllers** that are arranged in a hierarchy or master-slave combination.
  Fig. 1 is a high-level schematic block diagram of a SoC that includes a pair of IP cores, **each** having associated **TAP controller**/JTAG

circuitry, and the logic and external connections for switching between each of the pair...

...without adding additional pins to the integrated circuit. Various embodiments of the present invention allow multiple TAP controllers on a single integrated circuit to be accessed in a controlled manner through a single TAP controller by including a bit in a data register of each of the TAP controllers, along with simple combinational logic. Addition of such user data registers is allowed in accordance...

...of the present invention allow a programmable switch from a default TAP controller to a second TAP controller. In this way the state of a SoC, as observed from outside the SoC, is...

...system). More complex embodiments allow for arrangements such as switching back and forth between individual TAP controllers; and daisy-chaining all the TAP controllers together.
An application of the present invention is to provide access to multiple TAP controllers on a single chip while complying with the standard set forth in the IEEE 1149.1 specification. In turn, each TAP controller controls the test-logic (e.g., boundary scan testing) or the debug features of an...

...of this illustrative embodiment of the present invention. The outputs of each of the one bit switch registers 212 are coupled to an XOR gate 214 to produce the mode signal 216...

...and corresponding mode pin, shown in Fig. 1.
In accordance with the present invention, the two TAP controllers will appear to be one TAP controller to an off-chip observer, such as a ...

...in the art.
Fig. 6 illustrates a process flow in accordance with the present invention. Switch register bits in two or more TAP controllers are reset 602 to a known state...

...illustrative embodiment having three TAP controllers (referred to as TAP1, TAP2, and TAP3) is described. Each TAP controller has a 1-bit switch register that resets to zero. Instead of using a single XOR to make the mode bit (as described above in connection with the example having two TAP controllers), a mode bus is used.
With respect to switching between TAP1, TAP2, and TAP3, assume a round-robin scheduling algorithm is implemented to provide access between all the TAP controllers. (It is noted that selecting one out of many TAPs is a different function than...

...as TAP1 to TAP4 in this example) is described.
With respect to switching between the various TAP controllers, assume round-robin scheduling is implemented between all TAP controllers. In this illustrative embodiment TAP1 is selected by default. When the switch register of the...

...The logic for the mode-bus is solely dependent on the value of the four switch register bits, S1, S2, S3 and S4, as shown in TABLE 4.
It is noted that there...

...driven by an individual selected TAP controller (using an n-to-1 multiplexer), or, if all TAP controllers are daisy-chained, the TDO is driven by the TDO signal from the...

...of a plurality of TAP controllers, along with straightforward combinational glue logic, the plurality of TAP controllers can be accessed without the need for additional chip pins, and without the need for additional TAP controllers. By adding a second bit to at least one of the TAP controllers, internal derivation of signals suitable for controlling desirable functionality of the plurality of TAP controllers can be achieved. Toggling the state of the added bits in the respective data registers of the plurality of TAP controllers provides the control information for either switching or daisy-chaining of the plurality of TAP controllers.
It is to be understood that the present invention is not limited to the

embodiments...

...CLAIMS B1
1. A method of coupling a **plurality** of test access port, TAP, controllers (102, 106) that each comprise a one-bit register...

...terminal (TDI) to an input terminal of the selected one of the plurality of TAP **controllers** (102, 106); and

e) coupling an output terminal (TDO) of the selected one of the **plurality** of **TAP controllers** (102, 106) to an external output terminal;

characterized by producing the first signal (216) based...

...least in part, on the state of the first register bit in each of the **plurality** of **TAP controllers** (102,106).
2. The method of Claim 1, wherein each TAP controller (102, 106) comprises...

...Claim 2, further comprising toggling the first register bit in the selected one of the **plurality** of **TAP controllers** (102, 106); and repeating steps b) through e).
4. The method of Claim 3, further...

...a test mode selection signal (104), and a test reset signal to each of the **plurality** of **TAP controllers** (102, 106).
5. The method of Claim 3, wherein the **plurality** of **TAP controllers** (102, 106) are disposed on a single integrated circuit.
6. The method of Claim 5...

...integrated circuit, a clock signal.
8. An integrated circuit, comprising: a plurality of functional blocks, **each** functional block having a **test access port**, **TAP controller** (102, 106) coupled thereto; **each TAP controller** (102, 106) including a one-bit register (212) for storing a first register bit, each...

...to produce a known output state in response to a reset signal, each first register **bit** further adapted to **toggle** in response to a register write operation; and

routing logic (214) adapted to selectively provide...

15/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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01374353
CAPTURING OF A REGISTER VALUE TO ANOTHER CLOCK DOMAIN
ERFASSUNG EINES REGISTERWERTES ZU EINEM ANDEREN TAKTBEREICH
CAPTURE D'UNE VALEUR DE REGISTRE DESTINEE A UN AUTRE DOMAINE D'HORLOGE
PATENT ASSIGNEE:
Sun Microsystems, Inc., (2616592), 4150 Network Circle, Santa Clara, California 95054, (US), (Proprietor designated states: all)
INVENTOR:
SMITH, Brian, L., 1152B La Rochelle Terrace, Sunnyvale, CA 94089, (US)
SCHULZ, Jurgen, M., 3439 Virgil Circle, Pleasanton, CA 94588, (US)
LEGAL REPRESENTATIVE:
Harris, Ian Richard (72231), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 1277112 A2 030122 (Basic)
EP 1277112 B1 030917
WO 2001082081 011101
APPLICATION (CC, No, Date): EP 2001928878 010425; WO 2001US13397 010425
PRIORITY (CC, No, Date): US 557987 000425
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS (V7): G06F-011/00

NOTE:
  No A-document published by EPO
LANGUAGE (Publication, Procedural, Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
      CLAIMS B (English) 200338 1051
      CLAIMS B (German) 200338 1137
      CLAIMS B (French) 200338 1157
      SPEC B (English) 200338 4390
Total word count - document A 0
Total word count - document B 7735
Total word count - documents A + B 7735

...SPECIFICATION address register 16, which may be at least enough bits to specify an address for **each** of the CSRs). **More** particularly, the JTAG **TAP controller** 12 may assert the Shift(underscore)AR signal to address register 16, which may then...

15/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00777909
TEST APPARATUS/METHOD FOR LEVEL SENSITIVE SCAN DESIGNS
PRUFVERFAHREN UND VORRICHTUNG FUR PEGELEMPFINDLICHE ABFRAGEKONSTRUKTIONEN
EQUIPEMENT ET PROCEDE DE CONTROLE POUR LES DISPOSITIFS DE SCANNAGE SENSIBLES AUX NIVEAUX
PATENT ASSIGNEE:
  CRAY RESEARCH, INC., (578485), 655A Lone Oak Drive, Eagan, Minnesota 55121, (US), (Proprietor designated states: all)
INVENTOR:
  WEST, Jeffrey, D., 1948 Declaration Drive, Eau Claire, WI 54703, (US)
LEGAL REPRESENTATIVE:
  Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. High Holborn 2-5 Warwick Court, London WC1R 5DJ, (GB)
PATENT (CC, No, Kind, Date): EP 792486 A1 970903 (Basic)
                              EP 792486 B1 000412
                              WO 9615495 960523
APPLICATION (CC, No, Date): EP 95923926 950616; WO 95US7672 950616
PRIORITY (CC, No, Date): US 340238 941116
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS (V7): G06F-011/267; G01R-031/28
NOTE:
  No A-document published by EPO
LANGUAGE (Publication, Procedural, Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
      CLAIMS B (English) 200015 559
      CLAIMS B (German) 200015 424
      CLAIMS B (French) 200015 726
      SPEC B (English) 200015 5032
Total word count - document A 0
Total word count - document B 6741
Total word count - documents A + B 6741

...SPECIFICATION state transitions, but do cause other actions within the boundary scan test logic. There are **two** paths through the **TAP controller** state machine. The first path controls the loading of the instruction register. This path is...

...load a chosen data register with data input at the test data input TDI. These **tap controller** states are suffixed with "-DR" **Each** of these paths serve the same purpose, but for **different** registers. This **TAP controller** state machine, including utilization of TRST, operates in accordance with the IEEE/ANSI standard for...

15/3,K/7 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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01565874
Selective tap initialization in a multicarrier equaliser
Selektive Tapfwertinitialisierung in einem Mehrtragerentzerrer
Initialisation selective de prise dans un egaliseur multiporteuse
PATENT ASSIGNEE:
  Thomson Licensing, (7064730), 46, quai Alphonse Le Gallo, 92100 Boulogne-Billancourt, (FR), (Applicant designated States: all)
INVENTOR:
  Belotserkovsky, Maxim B., Thomson multimedia, 46, Quai Alphonse Le Gallo, 92648 Boulogne Billancourt Cedex, (FR)
  Litwin, Louis Robert, Jr., Thomson multimedia, 46, Quai Alphonse Le Gallo, 92648 Boulogne Billancourt Cedex, (FR)
LEGAL REPRESENTATIVE:
  Kohrs, Martin (88662), Thomson multimedia 46, quai A. Le Gallo, 92100 Boulogne-Billancourt, (FR)
PATENT (CC, No, Kind, Date): EP 1303092 A2 030416 (Basic)
                             EP 1303092 A3 060712
APPLICATION (CC, No, Date): EP 2002019906 020904;
PRIORITY (CC, No, Date): US 955651 010919
DESIGNATED STATES: AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; SK; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS (V7): H04L-025/03
INTERNATIONAL CLASSIFICATION (V8 + ATTRIBUTES):
IPC + Level Value Position Status Version Action Source Office:
  H04L-0025/03 A I F B 20060101 20030118 H EP
ABSTRACT WORD COUNT: 156
NOTE:
  Figure number on first page: 3

LANGUAGE (Publication, Procedural, Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
      CLAIMS A (English) 200316 851
      SPEC A (English) 200316 4273
Total word count - document A 5125
Total word count - document B 0
Total word count - documents A + B 5125

...SPECIFICATION for selective re-initialization mode 600. For example, when the predetermined time limit is 2 **seconds**, then **tap** initialization **controller** 108 responds to a time of 1.9 seconds between the end of one transmission...
...the next in a like manner as its response to a time of 0.1 **seconds** (in **both** cases, **tap** initialization **controller** 108 causes OFDM receiver 20 to operate according to selective re-initialization mode 600). Thus...

15/3,K/8 (Item 8 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00918245
A method and apparatus for scan testing of electrical circuits
Verfahren und Vorrichtung zur Boundary-scan Prufung von elektrischen Schaltungen
Procede et appareil de test de boundary-scan pour circuits electriques
PATENT ASSIGNEE:
  TEXAS INSTRUMENTS INC., (279076), 13500 North Central Expressway, Dallas, Texas 75243, (US), (Proprietor designated states: all)
INVENTOR:
  Whetsel, Lee D., 512 Bullingham Lane, Allen, Texas 75002, (US)
LEGAL REPRESENTATIVE:
  Meldrum, David James (127431), D Young & Co 120 Holborn, London EC1N 2DY (GB)
PATENT (CC, No, Kind, Date): EP 837336 A2 980422 (Basic)
                             EP 837336 A3 990512
                             EP 837336 B1 051214
APPLICATION (CC, No, Date): EP 97308297 971020;
PRIORITY (CC, No, Date): US 28821 P 961018
DESIGNATED STATES: DE; FR; GB; IT; NL

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INTERNATIONAL PATENT CLASS (V7): G01R-031/3185
ABSTRACT WORD COUNT: 14002
NOTE:
  Figure number on first page: 7

LANGUAGE (Publication, Procedural, Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text  Language    Update     Word Count
      CLAIMS B  (English)  200550          95
      CLAIMS B  (German)   200550          82
      CLAIMS B  (French)   200550         117
      SPEC B    (English)  200550       13440
Total word count - document A              0
Total word count - document B          13734
Total word count - documents A + B     13734

...SPECIFICATION operation would then immediately follow the update
  operation. A similar situation arises if the conventional IEEE 1149.1
  TAP controller is used to control the warping scan path. The TAP
  controller outputs control for capture-shift-update sequences. Thus,
  the TAP controller will also insert an update operation after each
  shift operation in Examples 1-7. Again, the update operation will not
  affect the operation...


 15/3,K/9      (Item 9 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2008 European Patent Office. All rts. reserv.

00656203
Method and apparatus for interference cancellation and adaptive
    equalisation in diversity reception
Verfahren und Vorrichtung zur Interferenzunterdruckung und adaptiven
    Entzerrung bei Diversityempfang
Procede et dispositif pour suppression d'interference et d'egalisation
    adaptative en reception de signaux en diversite
PATENT ASSIGNEE:
  NEC CORPORATION, (236690), 7-1, Shiba 5-chome, Minato-ku, Tokyo, (JP),
    (Proprietor designated states: all)
INVENTOR:
  Tsujimoto, Ichiro, c/o NEC Corporation, 7-1 Shiba 5-chome, Minato-ku,
    Tokyo, (JP)
LEGAL REPRESENTATIVE:
  Garratt, Peter Douglas (43121), Mathys & Squire 100 Grays Inn Road,
    London WC1X 8AL, (GB)
PATENT (CC, No, Kind, Date):   EP 631399   A1  941228 (Basic)
                               EP 631399   B1  020313
APPLICATION (CC, No, Date):    EP 94304600 940624;
PRIORITY (CC, No, Date): JP 93155439 930625
DESIGNATED STATES: FR; GB; IT
INTERNATIONAL PATENT CLASS (V7): H04B-007/005
ABSTRACT WORD COUNT: 153
NOTE:
  Figure number on first page: 2

LANGUAGE (Publication, Procedural, Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text  Language    Update     Word Count
      CLAIMS A  (English)  EPABF2        1182
      CLAIMS B  (English)  200211         896
      CLAIMS B  (German)   200211         802
      CLAIMS B  (French)   200211        1012
      SPEC A    (English)  EPABF2        6000
      SPEC B    (English)  200211        5996
Total word count - document A          7183
Total word count - document B          8706
Total word count - documents A + B    15889

...SPECIFICATION 1). In response to the first error signal (epsilon)(sub
  1), the first and the second tap gain controllers 103 and 104
  adjust each tap factor of the first and the second transversal filtered
  signals S( sub(f1)) and...
```

...SPECIFICATION epsilon))). In response to the first error signal (epsilon))' the first and the **second tap** gain **controllers** 103 and 104 adjust **each** tap factor of the first and the second transversal filtered signals Sf1)) and Sf2)). The...

15/3,K/10 (Item 10 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2008 WIPO/Thomson. All rts. reserv.

01084075 **Image available**
HIERARCHICAL TEST METHODOLOGY FOR MULTI-CORE CHIPS
METHODOLOGIE DE TEST HIERARCHIQUE POUR PUCES A NOYAUX MULTIPLES
Patent Applicant/Assignee:
SUN MICROSYSTEMS INC, 4150 Network Circle, Santa Clara, CA 95054, US, US (Residence), US (Nationality)
Inventor(s):
PENDURKAR Rajesh Y, 555 East Washington Avenue, Apt. 805, Sunnyvale, CA 94086, US,
Legal Representative:
PENILLA Albert S (agent), Martine & Penilla, LLP, 710 Lakeway Drive, Suite 170, Sunnyvale, CA 94085, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200405949 A1 20040115 (WO 0405949)
Application: WO 2003US21101 20030702 (PCT/WO US2003021101)
Priority Application: US 2002189870 20020703
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE SI SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 6311

Fulltext Availability:
Detailed Description

Detailed Description
... for simplicity). For one embodiment, TMS and TCK are provided to TAP controller 502 of **each** core 500 simultaneously so that **all** core **TAP controllers** 502 are in the same state. For another embodiment, TMS and TCK are provided to **each** core **TAP controller** 502 by chip MBC 304, which in turn may independently transition the states of **various** core **TAP controllers** 502, for example, when scheduling sequential BIST operations for selected cores 500.
Core MBC 504...

15/3,K/11 (Item 11 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2008 WIPO/Thomson. All rts. reserv.

00954679 **Image available**
METHOD AND CIRCUIT FOR TESTING HIGH FREQUENCY MIXED SIGNAL CIRCUITS WITH LOW FREQUENCY SIGNALS
PROCEDE ET CIRCUIT PERMETTANT DE TESTER DES CIRCUITS DE SIGNALISATION HAUTE FREQUENCE MIXTES A L'AIDE DE SIGNAUX BASSE FREQUENCE
Patent Applicant/Assignee:
LOGICVISION INC, 101 Metro Drive, Third Floor, San Jose, CA 95110, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
SUNTER Stephen K, 118 Arbeatha Street, Ottawa, Ontario K2H 6J2, CA, CA (Residence), CA (Nationality), (Designated only for: US)

Legal Representative:
PROULX Eugene E (agent), LogicVision (Canada), Inc., 1525 Carling Avenue, Suite 404, Ottawa, Ontario K1Z 8R9, CA,
Patent and Priority Information (Country, Number, Date):
Patent: WO 2002088759 A1 **20021107** (WO 0288759)
Application: WO 2002US12273 20020419 (PCT/WO US0212273)
Priority Application: US 2001842700 20010427
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English

Filing Language: English
Fulltext Word Count: 10730

Patent and Priority Information (Country, Number, Date):
Patent: ... **20021107**
Fulltext Availability:
Detailed Description
Publication Year: **2002**

Detailed Description
... by the TAP and the logic values in update latches 286 and 288, respectively. The **switches** are enabled by loading a **switch** enabling bit, logic 1, into their associated update latches.
- 20 0082 FIG. 8A illustrates a circuit 300 that combines a sampling clock 302 with the **TAP controller** output signal, ModeZ common to all the ABIVIs, one or more of which operate like an ABIVI constructed according to the...

15/3,K/12 (Item 12 from file: 349)
DIALOG(R)File 349: PCT FULLTEXT
(c) 2008 WIPO/Thomson. All rts. reserv.

00918286 **Image available**
METHOD FOR SCAN CONTROLLED SEQUENTIAL SAMPLING OF ANALOG SIGNALS AND CIRCUIT FOR USE THEREWITH
PROCEDE D'ECHANTILLONNAGE SEQUENTIEL COMMANDE PAR BALAYAGE DE SIGNAUX ANALOGIQUES ET CIRCUIT A CET EFFET
Patent Applicant/Assignee:
LOGICVISION INC, 101 Metro Drive, Third Floor, San Jose, CA 95110, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
SUNTER Stephen K, 118 Arbeatha Street, Ottawa, Ontario K2H 6J2, CA, CA (Residence), CA (Nationality), (Designated only for: US)
Legal Representative:
PROULX Eugene E (agent), LogicVision (Canada), Inc., 1525 Carling Avenue, Suite 404, Ottawa, Ontario K1Z 8R9, CA,
Patent and Priority Information (Country, Number, Date):
Patent: WO 2002052289 A1 **20020704** (WO 0252289)
Application: WO 2001CA1683 20011129 (PCT/WO CA0101683)
Priority Application: CA 2329597 20001222
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English
Filing Language: English
Fulltext Word Count: 7462

Patent and Priority Information (Country, Number, Date):
Patent: ... **20020704**
Fulltext Availability:
Detailed Description
Claims

Publication Year: **2002**

Claim
... the signal nodes;
generating a second update signal for each boundary module that controls analog **switches** ; and
applying a programmable register **bit** for controlling whether, during an UpdateDR state of said TAP controller, the first and second...

...1149.4
compatible mixed-signal circuit having analog busses for accessing said signal nodes, a **test access port controller** , an analog boundary module associated with **each** said circuit node, each module having shift register elements, associated update latches, a pair of...

15/3,K/13 (Item 13 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2008 WIPO/Thomson. All rts. reserv.

00908922 **Image available**
MULTIPLE DEVICE SCAN CHAIN EMULATION/DEBUGGING
EMULATION/DEBOGGAGE DANS UNE CHAINE DE REGISTRE AVEC DE MULTIPLES DISPOSITIFS
Patent Applicant/Assignee:
WIND RIVER SYSTEMS INC, 500 Wind River Way, Alameda, CA 94501, US, US (Residence), US (Nationality)
Inventor(s):
O'BRIEN James J, 4 Town Way, Hull, MA 02045, US,
Legal Representative:
SAMPSON Richard L (agent), Sampson & Associates, P.C., 50 Congress Street, Boston, MA 02109, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200242949 A1 **20020530** (WO 0242949)
Application: WO 2001US48003 20011116 (PCT/WO US0148003)
Priority Application: US 2000252316 20001121; US 2001921250 20010802
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 7583

Patent and Priority Information (Country, Number, Date):
Patent: ... **20020530**
Fulltext Availability:
Detailed Description
Publication Year: **2002**

Detailed Description
... manner, i.e., by sending a predetermined signal to TMS line 1 00 to cause **each TAP controller** 8 6 to
issue control-signal values that place the devices into the data phase.)
The emulator 1 1 0 may then generate conventional emulation/debugging

commands, which are modified as described hereinabove to compensate for the bits added by the bypassed 1:0 devices 30', etc, as the bit stream passes between...

15/3,K/14 (Item 14 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2008 WIPO/Thomson. All rts. reserv.

00340738 **Image available**
CONTROLLER AND METHOD FOR CONTROLLING ELECTRICAL SUPERGRID TRANSFORMER VOLTAGE
CONTROLEUR ET PROCEDE DE REGULATION DE LA TENSION DES TRANSFORMATEURS DE RESEAUX HAUTE TENSION
Patent Applicant/Assignee:
THE FOXBORO COMPANY,
de SA Douglas,
MAALOUF Salim Ibrahim,
Inventor(s):
de SA Douglas,
MAALOUF Salim Ibrahim,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9623250 A1 **19960801**
Application: WO 96GB162 19960125 (PCT/WO GB9600162)
Priority Application: GB 951432 19950125
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
US AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 8341

Patent and Priority Information (Country, Number, Date):
Patent: ... **19960801**
Fulltext Availability:
Detailed Description
Claims

Publication Year: **1996**

Detailed Description
... changing transformers whose outputs are connected to a respective common busbar, the controller comprises.

a **plurality** of transformer **tap** position **controllers** **each** of which is associated with a respective transformer of the group of transformers and is...

Claim
... changing transformers whose outputs are connected to a respective common busbar, the controller comprising:
a **plurality** of transformer **tap** position **controllers** **each** of which is associated with a respective transformer of the group of transformers and is...

21/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2008 European Patent Office. All rts. reserv.

01553071
METHOD AND APPARATUS FOR OPTIMIZED PARALLEL TESTING AND ACCESS OF ELECTRONIC CIRCUITS
VERFAHREN UND VORRICHTUNG ZUR OPTIMIERTEN PARALLELEN PRUFUNG UND ZUM ZUGRIFF AUF ELEKTRONISCHE SCHALTUNG
PROCEDE ET APPAREIL DESTINES A L'ACCES ET AU TEST OPTIMISES, EN PARALLELE, DE CIRCUITS ELECTRONIQUES
PATENT ASSIGNEE:
  Intellitech Corporation, (3886540), 70 Main Street, Durham, NH 03824, (US), (Proprietor designated states: all)
INVENTOR:

  RICCHETTI, Michael, 54 Cathedral Circle, Nashua, NH 03063, (US)
  CLARK, Christopher, J., 22B Cedar Point Road, Durham, NH 03824, (US)
LEGAL REPRESENTATIVE:
  Thevenet, Jean-Bruno et al (39781), Cabinet Beau de Lomenie 158, rue de l'Universite, 75340 Paris Cedex 07, (FR)
PATENT (CC, No, Kind, Date): EP 1402278 A1 040331 (Basic)
                             EP 1402278 B1 070815
                             WO 2003005050 030116
APPLICATION (CC, No, Date): EP 2002742331 020627; WO 2002US20505 020627
PRIORITY (CC, No, Date): US 303052 P 010705; US 119060 020409
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS (V7): G01R-031/28
INTERNATIONAL CLASSIFICATION (V8 + ATTRIBUTES):
IPC + Level Value Position Status Version Action Source Office:
  G01R-0031/28 A I F B 20060101 20030121 H EP
  G01R-0031/3185 A I L B 20060101 20050331 H EP
NOTE:
  No A-document published by EPO
LANGUAGE (Publication, Procedural, Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
      CLAIMS B (English) 200733 1970
      CLAIMS B (German) 200733 1939
      CLAIMS B (French) 200733 2400
      SPEC B (English) 200733 17225
Total word count - document A 0
Total word count - document B 23534
Total word count - documents A + B 23534

...SPECIFICATION a stable state, or to communicate with the UUT via the ATL 602 while the two TAP Controllers operate in lock step.
    The TMS(underscore)CONTROL instruction selects the TMS(underscore)Control register, which is then loaded with a TMS control code from the test controller 502. Depending on the TMS control code that was loaded into the TMS(underscore)Control register, the TMS(underscore)UUT output of the ATL 602 is controlled in one of four...

21/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2008 European Patent Office. All rts. reserv.

01446300
A TEST ACCESS PORT (TAP) CONTROLLER SYSTEM AND METHOD TO DEBUG INTERNAL INTERMEDIATE SCAN TEST FAULTS
TESTZUGRIFFS-PORTSTEUERUNGSVORRICHTUNG (TAP) UND VERFAHREN ZUR BESEITIGUNG INTERNER INTERMEDIARER ABTASTPRUFFEHLER
SYSTEME ET PROCEDE DESTINES A UNE UNITE DE COMMANDE D'UN PORT D'ACCES POUR ESSAI (TAP) AUX FINS DE DEBOGAGE D'ERREURS D'ESSAI DE BALAYAGE INTERMEDIAIRES INTERNES
PATENT ASSIGNEE:
  Koninklijke Philips Electronics N.V., (200769), Groenewoudseweg 1, 5621

BA Eindhoven, (NL), (Proprietor designated states: all)
INVENTOR:
JARAMILLO, Kenneth, Prof. Holstlaan 6, NL-5656 AA Eindhoven, (NL)
VAJJHALA, Varaprasda, Prof. Holstlaan 6, NL-5656 AA Eindhoven, (NL)
LEGAL REPRESENTATIVE:
Duijvestijn, Adrianus Johannes et al (87281), Philips Intellectual Property & Standards P.O. Box 220, 5600 AE Eindhoven, (NL)
PATENT (CC, No, Kind, Date): EP 1236053 A2 020904 (Basic)
EP 1236053 B1 050420
WO 2002029568 020411
APPLICATION (CC, No, Date): EP 2001969807 011002; WO 2001EP11401 011002
PRIORITY (CC, No, Date): US 678412 001002
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
INTERNATIONAL PATENT CLASS (V7): G01R-031/3185
NOTE:
No A-document published by EPO
LANGUAGE (Publication, Procedural, Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS B (English) 200516 1111
CLAIMS B (German) 200516 1003
CLAIMS B (French) 200516 1347
SPEC B (English) 200516 5357
Total word count - document A 0
Total word count - document B 8818
Total word count - documents A + B 8818

...SPECIFICATION test signals or it is utilized to forward boundary scan test signals. Internal scan observe **register** 111 is an **additional** **TAP** **controller** data **register** that provides internal scan test directions to the output control circuit 112 when the TAP...

21/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2008 European Patent Office. All rts. reserv.

01566426
Dual mode ASIC BIST Controller
ASIC BIST Kontroller mit zwei Moden
Controleur avec deux modes pour un BIST dans un ASIC
PATENT ASSIGNEE:
Sun Microsystems, Inc., (2616592), 4150 Network Circle, Santa Clara, California 95054, (US), (Applicant designated States: all)
INVENTOR:
Dorsey, Michael C., 9450-B Mira Mesa Blvd. 350, San Diego, California, (US)
LEGAL REPRESENTATIVE:
Harris, Ian Richard et al (72231), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 1302777 A2 030416 (Basic)
EP 1302777 A3 040616
APPLICATION (CC, No, Date): EP 2002257073 021011;
PRIORITY (CC, No, Date): US 976554 011012
DESIGNATED STATES: DE; FR; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS (V7): G01R-031/3185; G01R-031/3187
ABSTRACT WORD COUNT: 141
NOTE:
Figure number on first page: 1

LANGUAGE (Publication, Procedural, Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) 200316 1386
SPEC A (English) 200316 5827
Total word count - document A 7213
Total word count - document B 0
Total word count - documents A + B 7213

...SPECIFICATION signature 140 are the contents of memory elements of the

BIST controller 100, such as **registers**, as is discussed further below. The controller 100 comprises a portion of an integrated circuit...

...ASIC') 150. The ASIC 150 includes a testing interface 180, preferably a Joint Test Action **Group** ("JTAG') **tap controller**, through which the BIST of the dual mode BIST controller 100 can be invoked and...

21/3,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2008 European Patent Office. All rts. reserv.

01200652
Apparatus for a power ring
Vorrichtung fur einen Powerring
Dispositif pour un anneau de puissance
PATENT ASSIGNEE:
Rheinmetall Landsysteme GmbH, (1317342), Falckensteiner Strasse 2, 24159 Kiel, (DE), (Proprietor designated states: all)
INVENTOR:
Johnke, Volker, Rosenweg 16, 24214 Gettorf, (DE)
Hernekamp, Christoph, Dr., Bulker Weg 14a, 24229 Strande, (DE)
LEGAL REPRESENTATIVE:
Dietrich, Barbara et al (63472), Rheinmetall AG Zentrale Patentabteilung Postfach 10 42 61, 40033 Dusseldorf, (DE)
PATENT (CC, No, Kind, Date): EP 1044851 A2 001018 (Basic)
EP 1044851 A3 010411
EP 1044851 B1 040915
EP 1044851 B1 040915
APPLICATION (CC, No, Date): EP 2000101548 000127;
PRIORITY (CC, No, Date): DE 19916452 990412
DESIGNATED STATES: DE; FR; GB; NL; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS (V7): B60R-016/02
ABSTRACT WORD COUNT: 53
NOTE:
Figure number on first page: 2

LANGUAGE (Publication, Procedural, Application): German; German; German
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (German) 200042 268
CLAIMS B (English) 200438 378
CLAIMS B (German) 200438 314
CLAIMS B (French) 200438 413
SPEC A (German) 200042 932
SPEC B (German) 200438 1080
Total word count - document A 1200
Total word count - document B 2185
Total word count - documents A + B 3385

...CLAIMS has a connection (5) and control nodes (2) as well as a number of controlled **switches** (3), **two** or **more tap controllers** (1.1, 1.2, 1.3, 1.4, 1.5) are connected in between in...

21/3,K/7 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2008 European Patent Office. All rts. reserv.

00877576
Automatic gain control
Automatische Verstarkungsregelung
Commande de gain automatique
PATENT ASSIGNEE:
SONY CORPORATION, (214025), 6-7-35 Kitashinagawa Shinagawa-ku, Tokyo 141, (JP), (applicant designated states: DE;FR;GB)
INVENTOR:
Haruta, Tsutomu, Intellectual Property Division, Sony Corporation, 6-7-35, Kitashinagawa, Shinagawa-ku, Tokyo 141, (JP)
Kumano, Kazuo, Intellectual Property Division, Sony Corporation, 6-7-35, Kitashinagawa, Shinagawa-ku, Tokyo 141, (JP)

LEGAL REPRESENTATIVE:
  Pilch, Adam John Michael et al (50481), D. YOUNG & CO., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 803977 A2 971029 (Basic)
                             EP 803977 A3 980520
APPLICATION (CC, No, Date): EP 97302628 970417;
PRIORITY (CC, No, Date): JP 96102299 960424
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS (V7): H03G-003/00; H03G-003/20; H03G-001/00;
ABSTRACT WORD COUNT: 122

LANGUAGE (Publication, Procedural, Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
      CLAIMS A (English) 9710WM 295
      SPEC A (English) 9710WM 2579
Total word count - document A 2874
Total word count - document B 0
Total word count - documents A + B 2874

...SPECIFICATION also to the input terminal of the filter 2.
    The decoder 5 decodes the 8- **bit** gain indicating digital signal outputted as a feedback control signal from the digital detector 4 and, depending on the decoded content, outputs a **switch** designation signal, which designates one **switch** to be turned on out of the entire M **switches** of the **switch group** 6, to a **tap controller** 6a of the **switch** group 6.
    The M on/off **switches** of the **switch** group 6 are controllable to be turned on or off individually by the tap controller 6a. More specifically, when the **switch** designation signal outputted from the decoder 5 designates the nth **switch**, the tap controller 6a turns on (connects) only the switch Sn)) out of the entire...

21/3,K/8 (Item 8 from file: 348)
DIALOG(R)File 348: EUROPEAN PATENTS
(c) 2008 European Patent Office. All rts. reserv.

00709425
System testing device and method using a JTAG circuit
Vorrichtung und Verfahren zum Testen eines Systems unter Verwendung eines JTAG-Schaltkreises
Dispositif et procede utilisant un circuit JTAG pour tester un systeme
PATENT ASSIGNEE:
  FUJITSU LIMITED, (211460), 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa 211, (JP), (Proprietor designated states: all)
INVENTOR:
  Kawano, Kayoko, c/o Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
  Takaki, Yasushi, c/o Fujitsu Limited, 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, (JP)
  Sutou, Shinichi, c/o Fujitsu Program, Laboratories Limited, 4-19, Shinyokohama 2-chome, Kouhoku-ku, Yokohama-shi, Kanagawa, 222, (JP)
  Hara, Kazuhiro, 908-18, Yabuhara, Kiso-mura, Kiso-gun, Nagano, 399-62, (JP)
LEGAL REPRESENTATIVE:
  Schmidt-Evers, Jurgen, Dipl.-Ing. et al (10439), Patentanwalte Mitscherlich & Partner, Sonnenstrasse 33, 80331 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 672910 A1 950920 (Basic)
                             EP 672910 B1 030604
APPLICATION (CC, No, Date): EP 95103342 950308;
PRIORITY (CC, No, Date): JP 9446706 940317
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS (V7): G01R-031/28; G01R-031/317
ABSTRACT WORD COUNT: 82
NOTE:
  Figure number on first page: 4

LANGUAGE (Publication, Procedural, Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
      CLAIMS A (English) EPAB95 879

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      CLAIMS B  (English)  200323      1107
      CLAIMS B  (German)   200323       998
      CLAIMS B  (French)   200323      1277
      SPEC A    (English)  EPAB95      5729
      SPEC B    (English)  200323      5738
Total word count - document A          6609
Total word count - document B          9120
Total word count - documents A + B    15729
...SPECIFICATION reaching the terminal of the LSI on the principle of a
   scan test.
     The bypass register 102 comprises a stage of shift register and
   enables an input from the test data input TDI to be bypassed to the test
   data output TDO. Accordingly, the bypass register 102 is used when data
   are bypassed from a JTAG circuit to another JTAG circuit.
     The TAP controller 107 shifts data to the instruction register
   104, the boundary scan register 101, or the bypass register 102 using
   the test mode selection input TMS and test clock input TCK. The data
   written to the instruction register 104 are input to the data register
    selector 103 to select either the boundary scan register 101 or the
   bypass register 102...

...The multiplexer 2 106 (MUX 2) selects and outputs an output signal from
   the instruction register 104, boundary scan register 101, or bypass
   register 102.
     Figure 2 shows the state transition of a test logic. The state
   transition of the test logic is controlled by the TAP controller 107 to
   realize various test states. The TAP controller 107 is controlled
   by the test mode selection input TMS, test clock input TCK, and...

...SPECIFICATION reaching the terminal of the LSI on the principle of a
   scan test.
     The bypass register 102 comprises a stage of shift register and
   enables an input from the test data input TDI to be bypassed to the test
   data output TDO. Accordingly, the bypass register 102 is used when data
   are bypassed from a JTAG circuit to another JTAG circuit.
     The TAP controller 107 shifts data to the instruction register
   104, the boundary scan register 101, or the bypass register 102 using
   the test mode selection input TMS and test clock input TCK. The data
   written to the instruction register 104 are input to the data register
    selector 103 to select either the boundary scan register 101 or the
   bypass register 102...

...The multiplexer 2 106 (MUX 2) selects and outputs an output signal from
   the instruction register 104, boundary scan register 101, or bypass
   register 102.
     Figure 2 shows the state transition of a test logic. The state
   transition of the test logic is controlled by the TAP controller 107 to
   realize various test states. The TAP controller 107 is controlled
   by the test mode selection input TMS, test clock input TCK, and...


 21/3,K/9      (Item 9 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00682287
Integrated microprocessor.
Integrierter Mikroprozessor.
Microprocesseur integre.
PATENT ASSIGNEE:
  ADVANCED MICRO DEVICES INC., (328124), One AMD Place, P.O. Box 3453,
    Sunnyvale, California 94088-3453, (US), (applicant designated states:
    BE; DE; DK; ES; FR; GB; GR; IE; IT; LU; NL; PT; SE)
INVENTOR:
  Magnusson, Hans L., 202 Caracara Drive, Buda, Texas 78610, (US)
  Gephardt, Douglas D., 8906 Romayne Lane, Austin, Texas 78748, (US)
  Mudgett, Dan S., 7610 Mifflin Kenedy Terrace, Austin, Texas 78749, (US)
LEGAL REPRESENTATIVE:
  Wright, Hugh Ronald et al (38051), Brookes & Martin 52/54 High Holborn,
    London WC1V 6SE, (GB)
PATENT (CC, No, Kind, Date):  EP 652516 A1  950510 (Basic)
APPLICATION (CC, No, Date):   EP 94307736 941021;
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PRICRITY (CC, No, Date): US 147695 931103
DESIGNATED STATES: BE; DE; DK; ES; FR; GB; GR; IE; IT; LU; NL; PT; SE
INTERNATICNAL PATENT CLASS (V7): G06F-011/00;
ABSTRACT WORD CCUNT: 195

LANGUAGE (Publication, Procedural, Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text   Language    Update     Word Count
      CLAIMS A   (English)   EPAB95      1379
      SPEC A     (English)   EPAB95     11501
Total word count - document A          12880
Total word count - document B              0
Total word count - documents A + B     12880

...SPECIFICATICN by clocking signal TCK.
    A test access port (TAP) controller 352 is coupled to shift register
  310 to control the transfer of input information from host 200 to HDT 15
  via...

...IEEE Standard Test Access Port (TAP) and Boundary-Scan Architecture,
  IEEE Std. 1149.1-1990.  More particularly, TAP controller 352 is a
  synchronous finite state machine which responds to changes in the TMS and
  ...


 21/3,K/10      (Item 10 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2008 European Patent Office. All rts. reserv.

00564013
Large-scale integrated circuit device
Hochintegriertes IC
Dispositif de circuit a haute densite d'integration
PATENT ASSIGNEE:
  NEC CORPCRATICN, (236690), 7-1, Shiba 5-chome, Minato-ku, Tokyo, (JP),
    (Proprietor designated states: all)
INVENTOR:
  Shoda, Masahiko, c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku,
    Toyko, (JP)
LEGAL REPRESENTATIVE:
  Glawe, Delfs, Moll & Partner (100692), Patentanwalte Postfach 26 01 62,
    80058 Munchen, (DE)
PATENT (CC, No, Kind, Date):  EP 565866  A2  931020 (Basic)
                              EP 565866  A3  971105
                              EP 565866  B1  020102
APPLICATICN (CC, No, Date):   EP 93103944 930311;
PRICRITY (CC, No, Date): JP 9263929 920319
DESIGNATED STATES: DE; FR; GB; IT
INTERNATICNAL PATENT CLASS (V7): G01R-031/3185
ABSTRACT WORD CCUNT: 206
NOTE:
  Figure number on first page: 1

LANGUAGE (Publication, Procedural, Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text   Language    Update     Word Count
      CLAIMS A   (English)   EPABF1       749
      CLAIMS B   (English)   200201       893
      CLAIMS B   (German)    200201       704
      CLAIMS B   (French)    200201      1114
      SPEC A     (English)   EPABF1      4867
      SPEC B     (English)   200201      4259
Total word count - document A          5616
Total word count - document B          6970
Total word count - documents A + B    12586

...SPECIFICATICN bus freezing signal 15, a reset signal 15 generated as one
  of a control signal group 216 by the TAP controller 201 (the same
  as the TAP controller 201 of Fig. 9) is used.
    The content...

...1, and illustrated in Fig. 2. Amongst, the reset signal 15 is adapted to
```

be switched from HIGH level to LOW level while the test mode select signal (TMS) 6 is...

...SPECIFICATION bus freezing signal 15, a reset signal 15 generated as one of a control signal group 216 by the TAP controller 201 (the same as the TAP controller 201 of Fig. 9) is used.
The content...

...1, and illustrated in Fig. 2. Amongst, the reset signal 15 is adapted to be switched from HIGH level to LOW level while the test mode select signal (TMS) 6 is...

21/3,K/11 (Item 11 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01210181 **Image available**
METHODS AND DEVICES FOR INJECTING COMMANDS IN SYSTEMS HAVING MULTIPLE MULTI-PROCESSOR CLUSTERS
PROCEDES ET DISPOSITIFS D'INJECTION DE COMMANDES DANS DES SYSTEMES POSSEDANT PLUSIEURS GROUPES DE MULTI PROCESSEURS
Patent Applicant/Assignee:
NEWISYS INC, 10814 Jollyville Road, Building 4, Suite 300, Austin, TX 78759, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
GURU Prasadh, 11111 Callanish Park Drive, Austin, TX 78750, US, US (Residence), US (Nationality), (Designated only for: US)
GLASCO David B, 10337 Ember Glen Drive, Austin, TX 78726, US, US (Residence), US (Nationality), (Designated only for: US)
KOTA Rajesh, 5817 Miramonte Drive, Austin, TX 78759, US, US (Residence), IN (Nationality), (Designated only for: US)
DIESING Scott, 8610 Columbia Falls Drive, Round Rock, TX 78681, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
SAMPSON Roger S (et al) (agent), Beyer Weaver & Thomas, LLP, P.O. Box 778, Berkeley, CA 94704-0778, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200517752 A1 20050224 (WO 0517752)
Application: WO 2004US22935 20040716 (PCT/WO US04022935)
Priority Application: US 2003635700 20030805
Designated States:
(All protection types applied unless otherwise stated - for applications 2004)
AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NA NI NO NZ OM PG PH PL PT RO RU SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PL PT RO SE SI SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) BW GH GM KE LS MW MZ NA SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 11676

Fulltext Availability:
Detailed Description

Detailed Description
... serial data path. In Capture IR state 344, status information is captured by the instruction register .

From a Capture state, TAP controller 321 enters either a Shift state or an Exit1 state. More commonly, TAP controller 321 enters a Shift state, enabling test data or status information to be shifted out...

21/3,K/12 (Item 12 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

01122514 **Image available**
BOUNDARY SCAN WITH STROBED PAD DRIVER ENABLE
REGISTRE A DECALAGE PERIPHERIQUE AVEC VALIDATION DE L'ETAGE D'ATTAQUE DE PLOT STROBEE
Patent Applicant/Assignee:
  LOGICVISION INC, 101 Metro Drive, Third Floor, San Jose, CA 95110, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
  SUNTER Stephen K, 118 Arbeatha Street, Ottawa, Ontario K2H 6J2, CA, CA (Residence), CA (Nationality), (Designated only for: US)
  GAUTHIER Pierre, 42 Croissant de la Paix, Aylmer, Quebec J9H 3X8, CA, CA (Residence), CA (Nationality), (Designated only for: US)
  NADEAU-DOSTIE Benoit, 17 Croissant de la Paix, Aylmer, Quebec J9H 3X7, CA, CA (Residence), CA (Nationality), (Designated only for: US)
Legal Representative:
  PROULX Eugene E (agent), LogicVision (Canada), Inc., 1525 Carling Avenue, Suite 404, Ottawa, Ontario K1Z 8R9, CA,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 200444601 A1 20040527 (WO 0444601)
  Application: WO 2003US35423 20031106 (PCT/WO US03035423)
  Priority Application: US 2002425994 20021114
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
  AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NI NO NZ OM PG PH PL PT RO RU SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW
  (EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE SI SK TR
  (OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
  (AP) BW GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
  (EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 5428

Fulltext Availability:
  Detailed Description

Detailed Description
... Mode, ClockDR, and UpdateDR signals to control the boundary scan cells which form boundary scan **register** 42. **Additional** TAP **controller** outputs include forceDisable, which may be the logic value of a bit in the Instruction **Register**.. Capture-DR which 5 indicates when the TAP controller is in its Capture-DR state...

21/3,K/13 (Item 13 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

01004437 **Image available**
CONFIGURABLE ASIC MEMORY BIST CONTROLLER EMPLOYING MULTIPLE STATE MACHINES
CONTROLEUR BIST A MEMOIRE A CIRCUIT INTEGRE SPECIFIQUE (ASIC) CONFIGURABLE UTILISANT DES MACHINES A ETATS MULTIPLES
Patent Applicant/Assignee:
  SUN MICROSYSTEMS INC, 4150 Network Circle, Santa Clara, CA 95054, US, US (Residence), US (Nationality)
Inventor(s):
  DORSEY Michael C, 9450-B Mira Mesa Blvd., #350, San Diego, CA 92126, US,
Legal Representative:
  KIVLIN B Noel (et al) (agent), Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C., P.O. Box 398, Austin, TX 78767-0398, US,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 200334440 A2 **20030424** (WO 0334440)
  Application: WO 2002US32058 20021007 (PCT/WO US0232058)
  Priority Application: US 2001976707 20011012
Designated States:
(Protection type is "patent" unless otherwise stated - for applications

prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ
EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR
LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI
SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LU MC NL PT SE SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 7550

Patent and Priority Information (Country, Number, Date):
Patent: ... **20030424**
Fulltext Availability:
Detailed Description
Publication Year: **2003**

Detailed Description
... 140 are the contents of memory elements of the BIST controller I 00, such as **registers**, as is discussed ftuther below.

The controller 100 comprises a portion of an integrated circuit...
...ASIC') 150. The ASIC 150 includes a testing interface 180, preferably a Joint Action Test **Group** ("JTAG") **tap controller**, through which the BIST of the dual mode BIST controller 1 00 can be invoked...

21/3,K/14 (Item 14 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01004436 **Image available**
MEMORY BIST EMPLOYING A MEMORY BIST SIGNATURE
AUTO-TEST INTEGRE DE MEMOIRE FAISANT APPEL A UNE SIGNATURE D'AUTO-TEST INTEGRE DE MEMOIRE
Patent Applicant/Assignee:
SUN MICROSYSTEMS INC, 4150 Network Circle, Santa Clara, CA 95054, US, US (Residence), US (Nationality)
Inventor(s):
DORSEY Michael C, 9450-B Mira Mesa Blvd., #350, San Diego, CA 92126, US,
Legal Representative:
KIVLIN B Noel (agent), Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C., P.O. Box 398, Austin, TX 78767-0398, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200334439 A2 **20030424** (WO 0334439)
Application: WO 2002US31883 20021007 (PCT/WO US0231883)
Priority Application: US 2001976701 20011012
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ
EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR
LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI
SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LU MC NL PT SE SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 7610

Patent and Priority Information (Country, Number, Date):
Patent: ... **20030424**
Fulltext Availability:
Detailed Description
Claims

Publication Year: **2003**

Detailed Description

... signature 140 are the contents of memory elements of the BIST controller 100, such as **registers**, as is discussed further below. The controller 100 comprises a portion of an integrated circuit...

...ASIC") 150. The ASIC 150 includes a testing interface 180, preferably a Joint Test Action **Group** ("JTAG") **tap** **controller**, through which the BIST of the dual mode

Claim

... integrated circuit device of claim 15, wherein the testing interface comprises a Joint Test Action **Group** **tap** **controller**.

23 ...logic built-in self-test and storing the results thereof, and a multiple input signature **register** capable of storing the results of an executed logic built-in self-test.